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(54) **Encoder, data detecting semiconductor integrated circuit applicable to the same and dynamic sense amplifier.**

(57) A encoder has a prefetch circuit or a flag data sense circuit built into the priority encoder provided for a CAM block. While a hit signal in the first priority subblock is being encoded, a hit signal in the second priority subblock can be stored in the prefetch circuit. Therefore, the encoding operation is performed without sub-block-to-subblock switch time and this makes the encoder best suitable for a large capacity CAM which is required to operate at high speed. Moreover, a semiconductor integrated circuit of the present invention detects the differential current between the current flowing through one signal line and the reference current flowing through the other signal line. Moreover, it can operate as the number detection circuit to detect the number of hit signal in the subblock, and it can operate as the timing control circuit to previously notify the encode termination of the hit signal in the subblock of the encoder described above. Therefore, this semiconductor integrated circuit can allow the encoder to encode very efficiently at high speed. Moreover, a dynamic sense amplifier is able to operate with a great operating margin.

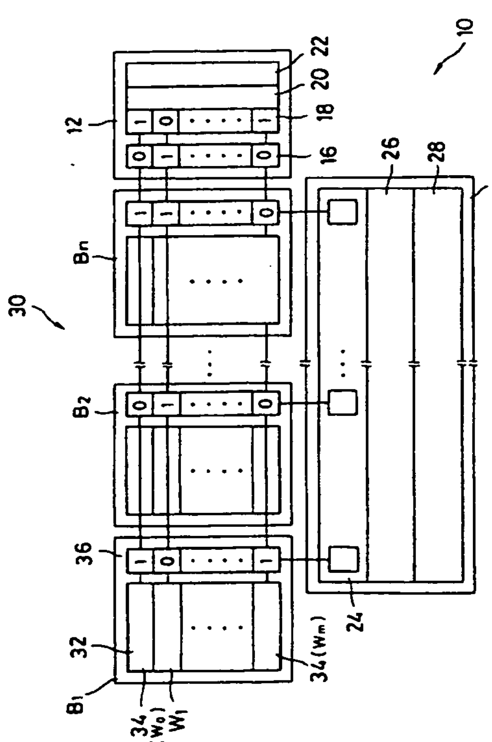

FIG. 1

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BACKGROUND OF THE INVENTION

The present invention relates generally to encoders, data detecting semiconductor integrated circuits applicable to such encoders and dynamic sense amplifiers, and more particularly to an encoder for sequentially efficiently encoding, in the order of predetermined priories, a plurality of match address signals from a number of blocks in a content addressable bulk memory and the like, a semiconductor integrated circuit for use in an encoder in the way of detecting the number of data which is increasing or decreasing as number of match addresses to be encoded is detected, and to a semiconductor integrated circuit provided with a dynamic differential current detection circuit for detecting a differential current existing in between a reference current line and a signal line and used for detecting the timing of terminating the operation of encoding a match address signal being encoded, together with a dynamic sense amplifier to be used for the purpose.

Heretofore, associative memories, that is, fully parallel CAMs (Content Addressable Memories), have been widely known as semiconductor storage circuits having the functions of performing the match detection of retrieval data and stored data concurrently in terms of all bits and outputting the match address of stored data or stored data (see "Design of CMOS VLSI," pp 176 - 177, edited by Tetsuya Iizuka and supervised by Takuo Sugano, Baifukan, 1989).
Content-addressed retrieval, instead of retrieval by means of physical memory addresses, is common to content addressable memories (CAMs). Therefore, the basic function of CAM, unlike an ordinary memory, is to input retrieval data so as to output a word address at which data matching the retrieval data has been stored.

However, only one word is not necessarily matching and there may be a plurality of them. When the plurality of match words are obtained like this, a correct encode output is unavailable with an ordinary encoder.

Consequently, CAM is equipped with a priority encoder for encoding and outputting a plurality of match (hit) signals in the order of predetermined priorities.

In a bulk CAM, however, the number of words is generally very large in contrast to the word length. For this reason, a cell array is divided into a plurality of blocks and it is an important problem how priority encoders are arranged. In other words, the priority encoders will occupy a large area and power consumption will also be on the increase if the priority encoder is provided for every block of CAM. As the number of blocks increases because of the division of the array, the area thus occupied thereby and the power consumption proportionally increase further.

As a result, there has been proposed a content addressable memory in which one main priority encoder is provided for the plurality of blocks and a block priority encoder to be separately provided is used for the block in which encoding is carried out by the main priority encoder.

Fig. 29 shows such a content addressable memory (CAM). As shown in Fig. 29, the content addressable memory 200 is divided into four CAM blocks 202 and each CAM block 202 is further divided into eight CAM subblocks 204. A priority encoder 210 is structurally hierarchical in that there are installed four main priority encoders 212, each being intended for the CAM block 202 having eight of the CAM subblocks 204, and one subblock priority encoder 214 is provided every four CAM blocks 202. As shown in Fig. 30, further, the CAM subblock 204 comprises a CAM subarray 206 having a predetermined number of CAM words with predetermined word length and its control unit including a hit signal register 208 for holding a hit signal resulting from the hitting of retrieval data against a CAM word.

At the time of match retrieval in the CAM block 202, the hit signals of all words in each subblock 204 are held by the hit signal register 208 and a subblock hit signal indicating the presence of a match word in the subblock 204 is simultaneously generated by an OR circuit (not shown) of the control unit in each CAM subblock 204. On receiving the signal, the subblock priority encoder 214 subsequently generates a subblock selection signal indicating the highest priority CAM subblock 204 and the subblock priority encoder 214 also generates an encoded subblock address. On receiving the block selection signal, a switch circuit (not shown) of the subblock thus selected is then activated to transfer the data (hit signal) held in the hit signal register 208 to the main priority encoder 212 as an output signal. Thereafter, the main priority encoder 212 generates a hit memory word address resulting from the hit signal thus transferred and encoded in the order of predetermined priorities in the CAM subblock 204. The priority encoder 210 combines the hit memory word address and the aforementioned subblock address and outputs the encoding logical address of the hit memory word of the CAM 200.

In the conventional CAM 200 shown in Figs. 29 and 30, the priority encoder (encoder) 210 comprises the main priority encoder (priority encoder) 212 for controlling the plurality of CAM subblocks 204 and the subblock priority encoder 214 for assigning priority to the CAM subblocks 204 for performing the encoding operation. The order of priorities is first determined among the plurality of the subblocks 204 and before being encoded, the output signal of the first priority subblock 204 is applied to the main priority encoder 212. The encoder can thus be made relatively small in configuration, whereas the circuit area relative to the whole circuit scale of the CAM 200 is reduced, whereby large scale integration is made fea-

sible.

Notwithstanding, subblock-to-subblock switch time becomes necessary until the encoding of the output signal (hit signal data (hereinafter called "flag data")) from the second priority CAM subblock 204 is started after the output signal (flag data) from the first priority subblock 204 is encoded by the main priority encoder 212 and output. In other words, it takes time to transfer the flag data from the hit signal register 208 of the second priority subblock 204 after an encoded address is output from the main priority encoder 212 and there still exists a problem arising from low encoding efficiency.

More specifically, there has been devised no encoder having the means of generating a signal for previously notifying or predicting the timing of terminating the operation of encoding flag data in the subblock (e.g., a termination notifying signal) and a signal for giving actual subblock-to-subblock flag data switch timing or the means of holding flag data in the second priority subblock at least until such a termination notifying signal is output in order to arrest the subblock-to-subblock switch time and to raise encoding efficiency in consideration of the switch time. Although a demand for a timing control circuit for detecting subblock-to-subblock switch timing is increasing, what is capable of outputting a switch timing notifying signal for previously notifying or predicting the termination of encoding the hit signal in the subblock (e.g., a termination notifying signal) stably with certainty has been nonexistent.

In this sense, a current difference detection circuit (sense amplifier) is used to compare a reference current for controlling the timing with the detected current so as to output the differential current. Although a differential current circuit of the static type has been mainly employed for the purpose, it still poses some problems one of which is that power consumption tends to increase because a steady state current flows therethrough and another one of which is that a relatively large area is needed for implementing a reference constant current circuit configuration.

BRIEF SUMMARY OF THE INVENTION

A first object of the present invention made to solve the foregoing problems in the prior art is to provide an encoder applicable to a content addressable bulk memory which is required to process mass data and provided with CAM blocks, each comprising a plurality of CAM subblocks, and which is capable of encoding output signals from a number of CAM subblocks continuously and efficiently with a predetermined cycle without subblock-to-subblock switch delay.

A second object of the present invention is to provide a semiconductor device applicable to an encoder of a content addressable bulk memory which is required to process mass data and provided with CAM blocks, each comprising a plurality of CAM subblocks, and which is capable of encoding output signals from the plurality of CAM subblock continuously and efficiently with a predetermined cycle without subblock-to-subblock switch delay to ensure that the timing of terminating the encoding operation being performed by the CAM subblock is detected stably beforehand with a high noise margin.

A third object of the present invention is to provide a semiconductor device capable of detecting the number of data in a data register by making a reference current control register hold the predetermined number of predetermined data and applicable to an encoder of a content addressable bulk memory which is required to process mass data and provided with CAM blocks, each comprising a plurality of CAM subblocks, and which is capable of encoding output signals from the plurality of CAM subblock continuously and efficiently with a predetermined cycle without subblock-to-subblock switch delay to ensure the detection of the fact that the number of uncoded flag data remaining in the CAM subblock performing the encoding operation has reached a predetermined value.

A fourth object of the present invention is to provide a dynamic sense amplifier capable of detecting not only the difference between current flowing through two signal lines, that is a potential difference resulting from the current difference, with low power consumption but also the timing of terminating the encoding operation to ensure that even when a number of loads are to be connected to the signal line or the difference between currents flowing through both signal lines, that is, the potential difference is small, it operates stably and accurately with a high noise margin.

In order to accomplish the first object by the first aspect of the present invention, there is provided an encoder for use in a content addressable memory having a plurality of content addressable memory subblocks, each having a plurality of content addressable memory words, the encoder comprising a priority main encoder for encoding flag data, in the order of predetermined priorities, resulting from matching with retrieval data fed to the plurality of memory words in the content addressable memory subblock, and a priority subblock encoder for assigning block-to-block priorities to the plurality of content addressable memory subblocks, the priority main encoder comprising a flag register for storing flag data to be encoded in the first priority content addressable memory subblock determined by said priority subblock encoder, and a prefetch circuit for prestoring flag data in the second priority content addressable memory subblock while the match signal in the flag register is being encoded.

In the first aspect, said encoder further compris-

es means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, and means for detecting the termination of the operation of encoding the match signal in the content addressable memory subblock, wherein the match signal applied to the prefetch circuit is encoded when the detection means detects the termination of the encoding operation therein.

There is provided by the second aspect of the present invention, in the first aspect, an encoder further comprising means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, and a timing detection control circuit for previously detecting the termination of the operation of encoding the match signal in the flag register and switching the flag data in the flag register over to the flag data in the prefetch circuit.

There is provided by the third aspect of the present invention an encoder for use in a content addressable memory having a plurality of content addressable memory subblocks, each having a plurality of content addressable memory words, the encoder comprising a priority main encoder for encoding flag data, in the order of predetermined priorities, resulting from matching with retrieval data fed to the plurality of memory words in the content addressable memory subblock, and a priority subblock encoder for assigning block-to-block priorities to the plurality of content addressable memory subblocks, the priority main encoder comprising a flag register for storing flag data to be encoded in the first priority content addressable memory subblock determined by said priority subblock encoder, means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, a timing circuit for previously detecting the termination of the operation of encoding the match signal in the flag register and controlling the timing at which flag data in the second priority content addressable memory subblock is prepared, and a flag data sense circuit for detecting from the content addressable memory word the flag data in the second priority content addressable memory subblock until the termination of the operation of encoding the match signal in the flag register .

Preferably, in the second and third aspects, the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of current drive means provided in parallel to the first signal line, M of data input lines connected to the flag register and receiving M of data for respectively controlling the current drive means, a second signal line, reference current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the current drive means and current flowing through the second signal line via the reference current drive means, wherein said number detection circuit is used for detecting the number of 0 or 1 in M of the data fed from M of the data input lines.

Preferably, the current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

Preferably, the signal voltage application transistor is provided between the control transistor and the first signal line.

Preferably, the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

Preferably, the timing circuit further comprises one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

Preferably, the timing circuit further comprises a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

Preferably, the timing circuit further comprises means for precharging the respective connections between the first and second transistors and the differential current detection means.

Preferably, the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of unit current drive means provided in parallel to the first signal line, data registers for respectively holding M of data for controlling the unit current drive means, a second signal line, N of reference unit current drive means provided in parallel to the second signal line, a reference current control register for holding N of data for controlling each reference unit current drive means, reference offset current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the unit current drive means and reference current flowing through the second signal line via N of the reference unit current drive means and the reference offset current drive means, wherein said number detection circuit is used for detecting the number of 0 or 1 in M of the data fed from

the data register to the unit current drive means in conformity with the number of 0 or 1 in N of the data held in the reference current control register.

In order to accomplish the second object by the fourth aspect of the present invention, there is provided a semiconductor integrated circuit comprising a first signal line, M (one or greater) of current drive means provided in parallel to the first signal line, M of data input lines for receiving M of data for respectively controlling the current drive means, a second signal line, reference current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the current drive means and current flowing through the second signal line via the reference current drive means, wherein

said semiconductor integrated circuit is used for detecting the number of 0 or 1 in M of the data fed from M of the data input lines. Preferably, in the fourth aspect, the current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

There is provided by the fifth aspect of the present invention, in the fourth aspect, a semiconductor integrated circuit wherein the signal voltage application transistor is provided between the control transistor and the first signal line.

There is provided by the sixth aspect of the present invention in the fourth or fifth aspect, a semiconductor integrated circuit wherein the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

There is provided by the seventh aspect of the present invention, in the above aspects, a semiconductor integrated circuit further comprising one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

There is provided by the eighth aspect of the present invention in the above aspects, a semiconductor integrated circuit further comprising a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

There is provided by the ninth aspect of the present invention, in the eighth aspect, a semiconductor integrated circuit further comprising means for precharging the respective connections between the first and second transistors and the differential current detection means.

In order to accomplish the third object by the tenth aspect of the present invention, there is provided a semiconductor integrated circuit comprising a first signal line, M (one or greater) of unit current drive means provided in parallel to the first signal line, data registers for respectively holding M of data for controlling the unit current drive means, a second signal line, N of reference unit current drive means provided in parallel to the second signal line, a reference current control register for holding N of data for controlling each reference unit current drive means, reference offset current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the unit current drive means and current flowing through the second signal line via N of the reference unit current drive means and the reference offset current drive means, wherein said semiconductor integrated circuit is used for detecting the number of 0 or 1 in M of the data fed from the data register to the unit current drive means in conformity with the number of 0 or 1 in N of the data held in the reference current control register.

In order to accomplish the fourth object by the eleventh aspect of the present invention, there is provided a dynamic sense amplifier comprising a first and a second signal line each having at least one detection node, first and second current drive means connected to the respective nodes of the first and second signal lines and having respective first and second input nodes corresponding to these signal lines, a current drive type latch circuit for detecting the differential current between the first and second signal lines, the latch circuit having a first output node and a second output node, and means for controlling the timing detected by the current drive type latch circuit, this means being provided between the current drive type latch circuit and the detection nodes of the first and second signal lines.

Preferably, a dynamic sense amplifier further comprises

a first conductive type first MOS transistor whose source is connected to a first supply potential node and whose drain is connected to the first output node, a second conductive type second transistor whose drain is connected to the first output node,

a first conductive type third MOS transistor whose source is connected to the first supply potential node and whose drain is connected to the second output node, and a second conductive type fourth transistor whose drain is connected to the second output node, wherein the gates of the first and second MOS transistors are simultaneously connected to the second output node, whereas the gates of the third and fourth MOS transistors are simultaneously con-

nected to the first output node, wherein the source of the second MOS transistor is connected to the first signal line, whereas the source of the fourth MOS transistor is connected to the second signal line.

Preferably, the first conductive type MOS transistor is a P- channel MOS transistor and wherein the second conductive type MOS transistor is an N-channel MOS transistor.

Preferably, the first conductive type MOS transistor is an N- channel MOS transistor and wherein the second conductive type MOS transistor is a P-channel MOS transistor.

Preferably, the first current drive means comprises a first signal transistor whose one electrode is connected to the detection node of the first signal line and whose gate is made the first input node, a second signal transistor whose one electrode is connected to the detection node of the second signal line and whose gate is made the second input node, and at least one control transistor connected between the other electrodes of the first and second signal transistors and the second supply potential node to receive a control signal at its gate.

Preferably, the at least one control transistor comprises a first control transistor connected between the first signal transistor and the second supply potential and a second control transistor connected between the second signal transistor and the second supply potential.

Preferably, the at least one control transistor is a transistor to be connected between the mutual source connection of the first and second signal transistors and the second supply potential.

Preferably, the detection timing control means is node potential setting means for setting the respective nodes of the first and second signal lines at a predetermined potential.

Preferably, the node potential setting means is precharge means.

Preferably, a dynamic sense amplifier further comprising detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

Preferably, the detection start level setting means is a first conductive type MOS transistor or a second conductive type MOS transistor provided between the current drive type latch circuit and the first supply potential node.

Preferably, the detection timing control means comprises a first and a second switch transistor, at least one first inverter provided between the gate electrode of the first switch transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second switch transistor and the second signal line.

Preferably, the detection timing control means is at least one inverter.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an encoder applicable to a content addressable memory according to the present invention.

Fig. 2 is a block diagram of a priority encoder with a prefetch circuit for use in the encoder according to the present invention.

Fig. 3 is a block diagram of a priority subblock encoder for use in the encoder according to the present invention.

Fig. 4 is a block diagram of a prefetch circuit for use in the encoder according to the present invention.

Fig. 5 is a block diagram of another priority circuit with encode circuits for use in the encoder according to the present invention.

Figs. 6(a), (b) and (c) are schematic block diagrams of small unit priority circuits for use in the priority circuit of Fig. 5 according to the present invention.

Fig. 7 is a block diagram of a logical arithmetic circuit for use in the small unit priority circuit of Fig. 5 according to the present invention.

Fig. 8 is a block diagram of another CAM block applicable to the encoder according to the present invention.

Fig. 9 is a block diagram of another priority encoder with a prefetch circuit for use in the encoder according to the present invention.

Fig. 10 is a timing control circuit as a semiconductor integrated circuit for use in the encoder according to the present invention.

Fig. 11 is a time chart showing timing in each portion of the priority circuit with a prefetch circuit for use in the encoder according to the present invention.

Fig. 12 is a block diagram of another timing control circuit as a semiconductor integrated circuit according to the present invention.

Fig. 13 is a time chart showing timing in each portion of the priority circuit with a prefetch circuit for use in the encoder to which the semiconductor integrated circuit is applied according to the present invention.

Figs. 14(a) and (b) are graphs showing the results detected by the timing circuits of Figs. 12 and 10, respectively.

Fig. 15 is a block diagram of another timing control circuit as a semiconductor integrated circuit according to the present invention.

Fig. 16 is a block diagram of still another timing control circuit as a semiconductor integrated circuit according to the present invention.

Figs. 17(a) and (b) are graphs showing the results detected by the timing circuits of Figs. 15 and 10, respectively.

Fig. 18 is a block diagram of still another timing control circuit to which the semiconductor integrated circuit is applied according to the present invention.

Fig. 19 is a block diagram of still another timing

control circuit to which the semiconductor integrated circuit is applied according to the present invention.

Fig. 20 is a block diagram of still another timing control circuit to which the semiconductor integrated circuit is applied according to the present invention.

Fig. 21 is a block diagram of still another timing control circuit to which the semiconductor integrated circuit is applied according to the present invention.

Fig. 22 is a block diagram of a priority subblock encoder component to which the semiconductor integrated circuit is applied according to the present invention.

Fig. 23 is a block diagram of still another timing control circuit as a semiconductor integrated circuit according to the present invention.

Fig. 24 is a block diagram of another CAM block applicable to an encoder according to the present invention.

Fig. 25 is a block diagram of another priority encoder for use in an encoder according to the present invention.

Fig. 26 is a block diagram of another timing control circuit to which a semiconductor integrated circuit for in the encoder is applied according to the present invention.

Fig. 27 is a timing chart explanatory of the function of the encoder according to the present invention.

Fig. 28 is a circuit diagram of a dynamic sense amplifier according to the present invention.

Fig. 29 is an overall block diagram of a content addressable memory employing a conventional encoder.

Fig. 30 is an overall block diagram of the content addressable memory employing the conventional encoder.

DETAILED DESCRIPTION OF THE INVENTION

The present invention will be described in detail further.

Referring to Figs. 1 - 7, a detailed description will first be given of an encoder in the first aspect of the present invention.

An encoder in the first aspect of the present invention is such that when retrieval data is fed to CAM blocks constituting a content addressable memory at the time of match retrieval, the match retrieval is made sequentially from the first one of a plurality of CAM subblocks. At this time, the result, that is, a signal (hit signal) matching the retrieval data is held in the plurality of CAM words on a CAM subblock basis. The highest priority CAM subblock is selected by a priority subblock encoder and then the hit signal is transferred to the priority encoder. The priority encoder encodes the hit signal and outputs a hit address. While the operation of encoding the hit signal is being performed, on the other hand, a hit signal in the second priority CAM subblock selected by the priority subblock encoder is applied to a prefetch circuit. The priority encoder starts to encode the hit signal in the second priority CAM subblock applied to the prefetch circuit immediately after the hit signal in the first priority CAM subblock has been encoded completely. Then a hit signal in the third priority CAM subblock is prefetched to the prefetch circuit having a free space. These steps are repeated successively to encode all hit signals in the whole CAM block, that is, to output addresses.

Since a hit signal to be subsequently encoded in the CAM subblock is applied to the prefetch circuit while the hit signal in the preceding CAM subblock is being encoded in the encoder as stated above, it is unnecessary to secure the time required to transfer the hit signal from the CAM subblock up to the priority encoder other than the encoding time. The encoding time to be taken by not only the whole CAM block but also the whole content addressable memory can thus be shortened, whereby the match retrieval operation can be performed by the content addressable memory at high speed.

Referring to the accompanying drawings, the encoder as a preferred embodiment in the first aspect of the present invention will subsequently be described.

Fig. 1 is a schematic diagram of the encoder applied to a CAM block in the first aspect of the present invention. As shown in Fig. 1, an encoder 10 according to the present invention comprises a priority encoder with a prefetch circuit (hereinafter called "main priority encoder" or "main encoder") 12, and a priority subblock encoder (hereinafter called "subblock priority encoder" or "subblock encoder") 14. The main encoder 12 comprises a prefetch circuit 16, a flag register circuit (or data latch circuit) 18, a priority circuit 20, and an encode circuit 22. The subblock encoder 14 comprises a latch circuit 24, a priority circuit 26, and an encode circuit 28.

The main encoder 12 is provided for a CAM block (hereinafter called "memory block") 30. The memory block 30 comprises a plurality (n pieces in Fig. 1) of CAM subblocks (hereinafter called "subblock") 32 (B_1, B_2,..., B_n). The subblock 32 comprises a subarray (CAM cell subarray) unit having a plurality (m+1 pieces in Fig. 1) of CAM words (hereinafter called "word") 34 (W_0, W_1,..., W_m) where a predetermined number of CAM memory cells are arranged in array, that is, where logical addresses with continuous predetermined word length are provided, registers 36 (R_1, R_2,..., R_n) for holding the result of match data retrieval in each word 34, for example, a match "1" signal (hit signal), a mismatch "0" signal in each word 34, and OR circuits for ORing the result of match retrieval (hereinafter called "flag data" or "hit signal data") in each word 34. The output of the OR circuit is held in the latch circuit 24 of the subblock encoder 14 to be described below on a subblock basis.

Fig. 2 is a block diagram of the main encoder 12. In Fig. 2, the prefetch circuit 16 of the main encoder 12 stores the hit signal data held in the register 36 of the second priority subblock 32 on a word 34 basis (W_0, W_1,..., W_m) while the priority circuit 20 and the encoder circuit 22 of the main encoder 12 are encoding the hit signal in the flag data in the first priority subblock 32 and the address of the match word 34 in the order of predetermined priorities. In this case, the prefetch circuit 16 may be any apparatus such as a data latch circuit or a data register as long as it is capable of temporarily holding m+1 of 1-bit data "0" or "1". After feeding the latch-held hit signal data of each word 34 to the data latch circuit 18 in parallel by means of the encode output (encode address output) of the main encoder 12, the prefetch circuit 16 fetches the hit signal data in the second priority subblock 32 selected by the subblock encoder 14 while the hit signal data is being encoded by the main encoder 12.

The data latch circuit 18 is used to latch-hold m+1 of 1-bit data like the prefetch circuit 16. While the priority circuit 20 selects data having the hit signal ("1") at one word address from the hit signal data of each word 34 (W_0, W_1,..., W_m), particularly what has a plurality of hit signals in the order of predetermined priorities, whereas the encode circuit 22 repeats the encoding operation, the data latch circuit 18 holds the hit signal data until all hit signals ("1") have been encoded. This data latch circuit 18 is so arranged that each time the hit signal ("1") at a high priority word address is encoded, the hit signal ("1") at that word address is reset. The flag register circuit 18 may be any apparatus as long as it can temporarily hold 1-bit data and therefore may be formed with a data latch circuit as previously noted, a data register or the like.

When hit signal data having a plurality of hit signals is applied as shown in Fig. 2, that is, on receiving m+1 of input signals of the whole word 34 having a plurality of match signals, the priority circuit 20 sequentially outputs an output signal including only one priority-ordered hit signal as designated in the order of predetermined priorities, thus including m+1 of priority circuit elements 40 (40_0, 40_1,..., 40_m). In this case, the second circuit element (hereinafter simply called "circuit element") 40_1 will be described as what represents the priority circuit elements 40 by way of example. The circuit element comprises an inverter 42 for inverting the input signal applied to the input terminal I_1, an N-channel MOS transistor 44 (N_1), a P-channel MOS transistor 46 (P_1), the output of the inverter 42 being connected to the gate electrodes of both transistors 44, 46 which are mutually exclusively controlled by the input signal, and a logical arithmetic circuit 48 with the source and drain electrodes of the NMOS transistor 44 as inputs and with the output terminal O_1 as an output.

One electrode (e.g., the source electrode) of the NMOS transistor N_1 is connected to the other electrode (e.g., the drain electrode) of the NMOS transistor N_0 of the high order circuit element 40_0 at a node Q_0, whereas the other electrode (e.g., the drain electrode) of the NMOS transistor N_1 is connected to one electrode (e.g., the source electrode) of the MOS transistor N2 of the low order circuit element 40_2 at a node Q_1. The NMOS transistors N_0, N_1, N_2,..., Nm are thus connected serially at nodes Q_0, Q_1, Q_2,..., Q_{m-1}. A node Q_m under the NMOS transistor N_m is connected to the OR output terminal $\underline{or}$ and this OR output terminal $\underline{or}$ is connected via an inverter 49 to each circuit of the prefetch circuit 16. Moreover, the electrode (e.g., the source electrode) above (on one side of) the uppermost stage NMOS transistor N0 is fixed to the potential (the signal state) indicating "0" or grounded. On the other hand, one electrodes (e.g., the source electrodes) of the respective PMOS transistors P_0, P_1, P_2,..., Pm are fixed to the potential (the signal state) indication "1" or connected to a power supply V_{pp}, whereas the other electrodes thereof (e.g., the drain electrodes) are connected to the respective nodes Q_0, Q_1, Q_2,..., Q_m. In this case, the direction of the connection of the electrodes (the source and drain electrodes) between the NMOS transistors may be reversed on condition that the NMOS transistors N_0, N_1, N_2,..., N_m are connected in series; the same will apply to the PMOS transistors P_0 - P_m. The priority circuit 20 having m+1 inputs and m+1 outputs is formed in this way.

A description will subsequently be given of the operation of assigning priority in the priority circuit 20, that is, the operation of outputting a priority-ordered output signal with only the first priority address as a match signal "1" even though a plurality of hit signals (match signals) "1" are applied from I_0 - I_m. When attention is directed to the circuit element 40_1 of the priority circuit 20, the N_1 transistor 44 is turned off and the P_1 transistor 46 is turned on if an I_1 input is 1. Therefore, the Q_1 node is set at 1 by the P_1 transistor 46. If an I_1 input is 0, the N_1 transistor 44 is turned on and the P_1 transistor 46 is turned off. Therefore, the Q_1 node becomes equal to the logical value of the Q_0 node higher by one level. If an I_k input is 1, Q_k becomes 1 and consequently $Q_j (j \geqq k+1)$ can be exclusively 1, irrespective of whether I_j is 1 or 0. In other words, (the signal state of) a node Q_{k+1} is 1 if $I_{k+1} = 1$ and $Q_{k+1} = Q_k$ if $I_{k+1} = 0$ and further $Q_{k+1} = 1$ from $Q_k = 1$.

As a result, with a plurality of I inputs being 1 in Fig. 2, "0" representing a propagation control signal is transmitted up to the NMOS transistor 44 located on the uppermost side while the corresponding serially-connected NMOS transistors 44 (N) remain off. However, the propagation control signal "0" is not transmitted to each lower Q node and 1 is retained in all the lower Q node. Consequently, the logical arithmetic circuit 48 may be used to detect the extent to which the control signal "0" has been transmitted. When all

m+1 inputs of I_0 - I_m of the priority circuit 20 become "0", the control signal "0" is transmitted up to the OR output terminal $\overline{or}$ and the absence of "1" in all m+1 input signals is made known. The termination of assigning priority to all the hit signals of the hit signal data in this subblock makes it known that the second priority hit signal data latch-held in the prefetch circuit 16 can be fed to the data latch circuit 18 and that the third priority hit signal data selected by the subblock encoder 14 can be written to the prefetch circuit 16 then.

As shown in Fig. 2, the logical arithmetic circuit 48 comprises an exclusive OR gate (mismatch circuit) 48a for exclusively ORing the signal state between the drain and source of the serially-connected NMOS transistor 44 (N_1), that is, the logical value between the nodes Q_0 and Q_1. In this logical arithmetic circuit 48, the propagation control signal "0" is propagated when the nodes Q_0 and Q_1 mismatch, that is, up to the node Q_0 of the NMOS transistor 44 (N_1) of the circuit element 40_1. When the propagation control signal "0" has not been propagated up to the node Q_1, however, the exclusive OR gate 48a outputs "1". When the nodes Q_0 and Q_1 match ("0"), the output of the output terminal O_1 is "0". The logical arithmetic circuit 48 is not limited in configuration to the example shown in Fig. 2 but may be so arranged as to perform desired logical operations with a combination of various gates. Moreover, the input of the logical arithmetic circuit 48 need not necessarily be applied between the nodes Q_0 and Q_1 but may be either one of them and an input signal or its inverted value and besides the contents of the logical operation may be selected properly in accordance with the signal value.

When the first priority-ordered output signal (O) having one hit signal is output from an input signal (I) having a plurality of hit signals, the first priority output signal should be used to reset the input side in a case where the address of the second priority match signal exists in the identical subblock 32. In other words, assuming $I_1 = 1$, $I_2 = 1$ in the priority circuit 20 of Fig. 2, for example, output $O_1 = 1$ since node $Q_0 = 0$, node $Q_1 = Q_2 =...= Q_m = 1$. If the O_1 output value is input to the reset terminal of the data latch circuit 18, $I_1 = 0$ and therefore the N transistor 44 (N_1) is turned on, whereas the P transistor 46 (P_1) is turned off, and node $Q_1 = Q_0 = 0$. Since the N transistor N_2 is held OFF, node $Q_0 = Q_1 = 0$, node $Q_2 =...= Q_m = 1$. The second priority $I_2 = 1$ is then selected as the next output signal.

The plurality of hit signals within the hit signal data in the identical subblock 32 are applied to the main encoder 12 at a time and the hit signals are sequentially applied to the encode circuit 22 by the priority circuit 20 as an output signal having only one hit signal in the order of predetermined priorities. Then "1" is applied to the reset terminal of the data latch circuit 18 of the word address corresponding to the "1" output and the hit signals ("1") latch-held in the data latch circuit 18 are sequentially reset. When the last priority-ordered hit signal is applied to the encode circuit 22 and applied to the encode circuit 22 before being reset, data "0" is transmitted to the lowermost node Qm of Fig. 2 before being output from the OR output terminal $\overline{or}$. Further, the data "0" is inverted by the inverter 49 and its inverted value "1" is applied to the whole data latch circuit 18. The hit signal data of the second priority subblock 32 latch-held in the prefetch circuit 16 is applied (shifted) to each corresponding circuit of the data latch circuit 18 and held therein. Moreover, the hit signal data in the third priority subblock 32 preselected by the subblock encoder 14 is read from the register 36 to the prefetch circuit 16 having a free space and latch-held. The priority circuit 20 thus terminates the processing of the hit signal data in the first priority subblock and since it need not wait for the hit signal data in the second priority subblock transferred from the register 36 of the subblock 32, it can perform the encoding operation with efficiency.

The encode circuit 20 is used to encode only one match signal address existing in the output signals sequentially output from the priority circuit 18 and to encode each word address at the output terminal O_0, O_1, O_2,..., O_m corresponding to each of the words 34 (W_0, W_1, W_2,..., W_m). The encode circuit 20 comprises L of address lines 50 (50_0, 50_1, 50_2,..., 50_{L-1}) for encoding L bits with respect of the smallest natural number L which comes up to $m+1 \leqq 2^L$, and a grounded transistor 52 affixed to each address line 50, whereas its gate electrode is connected to the output line from each of the output terminals O_0, O_1, O_2,..., O_m. In this case, one ends of the respective L address lines 50_0, 50_1, 50_2,..., 50_{L-1} are connected via respective resistors r_0, r_1, r_2,..., r_{L-1} to a power supply (or fixed to "1" potential) and the transistor 52 is so installed as to make L-bit code outputs of $A_{L-1}...A_2 A_1 A_0$ available.

The output line from the output terminal O_0, for example, is connected to all the gate electrodes of L of grounded transistors 52 connected to all L address lines 50_0 - 50_{L-1}. When the output of the output terminal O_0 is, for example, "1" (match signal) and when the remainder is all "0", $A_{L-1} =...= A_2 = A_1 = A_0 = 0$, thus indicating $(A_{L-1}...A_2 A_1 A_0) = (0...0\ 0\ 0)$. Subsequently, the output terminals O_1 and O_2 corresponding to the second and third word addresses W_1, W_2 are respectively connected to the gate electrodes of L pieces of the grounded transistors 52 connected to L-2 pieces of address lines 50_1 - 50_{L-1} and 50_0, 50_2 - 50_{L-1} excluding the address lines 50_0 and 50_1. Only when the output terminals O_1 and O_2 become "1", they respectively represent $(A_{L-1}...A_2 A_1 A_0) = (0...0\ 0\ 1)$ and $(0...0\ 1\ 0)$.

Thereafter, the grounded transistor 52 is connected to each address line 50 in such a way as to represent each code address likewise. When $m+1 = 2^L$, for ex-

ample, the output line of the last output terminal O_m is connected only the grounded transistor 52 fitted to the address line 50_{L-1} and only when the output terminal O_m is 1, it represents $(A_{L-1}...A_2 A_1 A_0) = (0\ 1...1\ 1\ 1)$ (the initial L digit represents 0 and the remainder L-1 all 1). When all output terminals $O_0, O_2,..., O_m$ is "0", it represents $(A_{L-1}...A_2 A_1 A_0) = (1...1\ 1\ 1)$ (all 1). The encode circuit 22 is basically thus arranged. The encode circuit 22 is limited to what has been illustrated but may be any other known circuit of the sort that is capable of encoding and outputting the "1" output address on receiving an input signal having the "1" output at only one word address. The main encoder 12 is basically thus configured.

Fig. 3 is a block diagram of the subblock encoder 14. As the data latch circuit 24, the priority circuit 26 and the encode circuit 28 shown in Fig. 3 are substantially similar in structure to the data latch circuit 18, the priority circuit 20 and the encode circuit 22 shown in Fig. 2 except that the number of units constituting each of them is m+1 instead of n, a detailed description of their circuit arrangements will be omitted. The result of match retrieval in each memory subblock 32, that is, hit signal data is held in the register 36 in the subblock encoder 14 at the time of match retrieval carried out in each CAM memory subblock 32 ($B_1, B_2,..., B_n$). Moreover, an OR circuit (not shown) in the subblock 32 causes a subblock hit signal indicating the presence or absence of the word 34 (hit word or match word) showing match retrieval data to be generated and held in the data latch circuit 24 of the corresponding subblock 32. Match retrieval is sequentially carried out in the subblock 32 and the block hit signal is latch-held in the data latch circuit 24 when the hit signal data is held in the register 36 of the relevant subblock 32.

On the other hand, the subblock 32 whose block hit signal latch-held in the data latch circuit 24 is the hit signal ("1") is selected in the order of predetermined priorities, from left to right in Fig. 3, in the priority circuit 26 of the subblock encoder 14 and the priority-ordered output signal having "1" at that block address is produced. The output signal is encoded and output by the following stage encode circuit 28 before being returned to the control unit of the relevant subblock 32. The gate circuit 54 in the control unit is then turned on and the hit signal data in the register 36 is fed to the fetch circuit 16 of the main encoder 12 after the fetch circuit 16 affords a free space. The subblock encoder 14 selects the priority subblock 32 to be encoded next in the order of predetermined priorities in this way and while the main encoder 12 is encoding the word address of the hit signal from the hit signal data in the first priority subblock 32, transfers the hit signal data in the second priority subblock 32 to the prefetch circuit 16 having a free space and has the data latch-held.

The encoder 10 according to the present invention combines the encoded block address output from the encode circuit 28 of the subblock encoder 14 and the encoded word address output from the encode circuit 22 of the main encoder 12 into an encoding logical address and sequentially output the result. When the last subblock 32 or the lowest priority subblock 32 is selected, the process in the subblock encoder 14 is terminated and when the operation of encoding whole hit signal by the main encoder is terminated, the encoder 10 outputs the hit signals of all memory words in the CAM subblock 30 as logical addresses and terminates the match retrieval operation. Although the encoder 10 having one main encoder 12 and one subblock encoder 14 with respect to the CAM block 30 having the plurality of CAM subblocks 32 has been referred to by way of example, the present invention is not limited to this example but may be so arranged as to have one subblock encoder 14 with respect to a plurality of CAM blocks 30 like a conventional encoder 210 applicable to the CAM 200 shown in Fig. 29.

Fig. 4 shows a specific circuit arrangement of the prefetch circuit 16 used in the encoder 10 according to the present invention together with a switch circuit 160 for controlling each subblock 32 required for the operation thereof and a precharge circuit 162.

A description will be given of one switch circuit 160 (S_0) connected to the register 36 (R_0) of a subblock 32 (B_1) by way of example. The switch circuit 160 (S_0) comprises two NMOS transistors 163, 164 connected in series. The electrode (e.g., the drain electrode) of one transistor 163 of each switch circuit 160 ($S_0, S_1,..., S_m$) is connected in parallel to a corresponding input line 165 ($L_0, L_1,..., L_m$) in each subblock 32 ($B_1, B_2,...B_n$), whereas a detection line L is connected to the prefetch circuit 16. The gate electrode of the transistor 163 of each switch circuit 160 ($S_0, S_2,...S_m$) is connected in parallel to a block selection line 167 and to an AND circuit 166. Moreover, the gate electrode of the other transistor 164 of each switch circuit 160 ($S_0, S_1,..., S_m$) is connected to the output terminal of the corresponding register 36 ($R_0, R_1,..., R_m$), whereas the other electrode (e.g., the source electrode) of the transistor 164 is grounded. Further, the precharge circuit 162 comprises a PMOS transistor 168 ($PC_0, PC_1,...PC_m$) as a precharge transistor for precharging the input line 165 ($L_0, L_1,..., L_m$) at a predetermined potential (e.g., power supply potential). One electrode of each PMOS 168 ($PC_0, PC_1,...PC_m$) is connected to a fixed potential source (power supply), the other electrode to the input line 165 ($L_0, L_1,..., L_m$) and the gate electrode to a precharge signal line 169.

The prefetch circuit 16 has (m+1) of data latch circuits, each comprising two invertors 170, 172 connected reversely in parallel and latch signal lines 174, 175 for receiving a control signal for controlling the output state of the invertors 170, 172. The input side

ends of the invertors 170, 172 connected in parallel are connected to the input line 165 (L_i), whereas the out side ends thereof are connected to circuit elements corresponding to the data latch circuit 118. Moreover, the latch signal line 174 is connected to the control signal terminal of the inverter 170 and the inverted control signal terminal of the inverter 172, whereas the latch signal line 175 is connected to the control signal terminal of the inverter 172 and the inverted control signal terminal of the inverter 170.

One input terminal of the AND circuit 166 is connected to a circuit element corresponding to the data latch circuit 24 (or the priority circuit 26) of the subblock encoder 14, whereas the other input terminal thereof is connected to a control signal line 176 for controlling the selection timing of the block selection line 167. The control signal line 176, the precharge signal line 169, the latch signal lines 174, 175 are connected to a timing control circuit for controlling the operative timing of each circuit.

The prefetch operation of the prefetch circuit 16 will subsequently be described.

First, all PMOS 168 (PC_0, PC_1,..., PC_m) are turned on with the precharge signal line 169 as L(low) and (m+1) of input lines 165 (L_0, L_1,..., L_m) of the prefetch circuit 116 are precharged at a predetermined potential. Subsequently, the timing control circuit 178 is operated to turn off (m+1) of PMOS 168 with the precharge signal line 169 as H. With the control line 176 as "1" (H) further, the block hit signal "1" of the second priority (the next priority of the subblock in which the main encoder 12 is performing the encoding operation) subblock 32 (B_i) with the block hit signal "1" latch-held in the data latch circuit 24 of the subblock encoder 14 is applied to the AND circuit 166. Then the block selection line 167 of the relevant subblock 32 (B_i) is turned on.

When the second priority subblock 32 (B_i) is selected so as to make the corresponding AND circuit 166 set the block selection line 167 at H (high level), the transistor 164 whose gate electrode has been connected to the register 36 (R_i) holding the hit signal ("1") out of the registers 36 and the transistor 163 connected thereto are turned on. These transistors 164, 163 operate to ground the input line 165 (L_i) and lower the potential of the input line by pulling out the precharged charge of the input line 165 (L_i). On the other hand, the transistor 164 whose gate has been connected to the register 136 (R_j) holding data of "0" (mismatch) is not turned on but remains off, whereby the potential of the corresponding input line 165 (L_j) is left unchanged even though the block selection line is set at H. The precharged potential is thus maintained.

Consequently, the potential of the input line 165 (L_0, L_1,..., L_m) varies with the value ("1": hit signal, "0": mishit signal) stored in the register 36 of the selected subblock 32 (B_i), thus inverting the polarity.

By giving the latch signal lines 174, 175 of the prefetch circuit 16 latch signals, the parallel-connected invertors 170, 172 of the prefetch circuit 16 are made to latch the signal. In this case, the input lines on the input side of the invertors 170, 172 become equal in polarity because their output sides are inverted, though these lines are opposite in polarity to the register 36. Consequently, the hit signal data in the next subblock 32 latched by the prefetch circuit 16 is fed to the data latch circuit 18 simultaneously when the encoding operation in the first priority subblock 32 of the main encoder 12 is terminated. Then the prefetch circuit 116 repeats the aforementioned operation in order to prefetch the hit signal data in the storage register 36 of the second priority subblock 32.

The encoder 10 according to the present invention is basically arranged like this.

The encoder 10 according to the present invention is not limited to what comprises the priority circuits 20, 26 and the encode circuit 22, 28 shown in Figs. 2, 3 but may employ heretofore known priority circuits and encode circuits or the priority circuit 180 and the encode circuit 190 shown in Figs. 5, 6 and 7 to speed up the operation of assigning priority and the encoding operation itself. Needless to say, the combination of the priority circuit 180 and the encode circuit 22 of Fig. 2 may be used in this case.

The priority circuit 180 shown in Fig. 5 has a ternary hierarchical structure: the lowest tier comprises sixteen 4-input small unit priority circuits (hereinafter called "unit circuits") 182; the intermediate tier comprises four similar 4-input small unit priority circuits 184; and the highest tier comprises one similar 4-input small unit priority circuit 186. Therefore, the priority circuit 180 is allowed to have 64 inputs because of sixteen unit circuits 182 in the lowest tier. In other words, 64 inputs of the priority circuit 180 are formed into 16 groups, each having four inputs. The small unit priority circuit 182 is formed with a group of four inputs and there are employed 16 small unit priority circuits. The 16 small unit priority circuits 182 are formed into four groups, one group comprising four unit circuits 182. The four unit circuits 182 constituting the one group are connected to one small unit priority circuit 184 forming the intermediate tier. Moreover, four of the unit circuits 184 are formed into a group and connected to the small unit priority circuits 186 in the highest tier.

The priority circuit 180 shown in Fig. 5 has 64 inputs and the ternary hierarchical structure with the 4-input unit circuits 182, 184 and 186 as component units. However, the present invention is not limited to this arrangement and there may be a hierarchical structure in which the number of elements in the respective unit circuits and that of hierarchical tiers are to be selected properly in proportion to the total number of inputs and the number of inputs in the respective unit circuits for use. Although the unit circuits 182, 184 and 186 constituting the respective hierarchical

tiers have been defined as those having the same number of inputs, the present invention is not limited to this arrangement but the number of inputs may vary. The smaller the number of inputs of the unit circuit, the more it is convenient to increase the priority variation rate. Nevertheless, an increase in the number of unit circuits required will result in an increase in the number of hierarchical tiers if the number of inputs of the unit circuit is too small and will further cause the number of accompanying elements and peripheral circuits to increase, which will be undesirable. Accordingly, the present invention suggests a multi-hierarchy structure in which the number of tiers should be determined properly by making selective the total number of inputs and the number of inputs of the unit circuit (either exclusive or multi-kind) usable in each hierarchical tier.

As shown in Fig. 6(a), the small unit priority circuit 182 is arranged in the order of ascending priorities and has four input units I_0, I_1, I_2 and I_3, four output terminals O_0, O_1, O_2 and O_3, an enable signal input terminal e, an OR output terminal or, and four priority circuit elements 188 (188_0, 188_1, 188_2 and 188_3). In this case, since the circuit element 188 is identical in configuration as the circuit element 40 of Fig. 2 except that the logical arithmetic circuit 48 used in the former has the enable signal input terminal e and is activated by the enable signal received therefrom, like component elements are designated by like reference characters and the description of them will be omitted.

Fig. 7 shows a specific exemplary configuration of the logical arithmetic circuit 48 of Fig. 6(a). The logical arithmetic circuit 48 shown in Fig. 7 comprises an exclusive OR gate 48a and an AND gate 48b for ANDing the output of the exclusive OR gate 48 and the enable signal e. The exclusive OR gate 48a of the logical arithmetic unit 48 output "1" when input signals mismatch, that is, when nodes Q_{I-1} and Q_I mismatch, whereas the AND gate 48b simultaneously applies "1" to the output terminal O_I when the enable signal e is "1" (active). The output terminal O_I is "0" when the input signals match or when the enable signal e is "0".

Figs. 6(b) and 6(c) are schematic diagrams of unit circuits 184 and 186 in the intermediate hierarchical tier and the highest hierarchical tier, respectively. As the unit circuits 184 and 186 shown in Fig. 6(b) and 6(c) have the same structure as that of the unit circuit 182 in the lowest tier shown in Fig. 6(a) except for the signals input to and output from the input/output signal terminals, the illustration of the arrangement thereof will be omitted. Input terminals or_0, or_1, or_2, or_3 of the unit circuit 184 shown in Fig. 6(b) are respective OR outputs or of the four unit circuits 182 forming the lowest hierarchical tier of Fig. 5. If the outputs O_{1k} (k = 0, 1, 2, 3) of the unit circuit 184 are connected to enable terminals e_k of the unit circuit 182_k corresponding to input signals or_k, No. k circuit 182_k can be activated selectively only when $O_{1k} = 1$. Therefore, the OR output may be used to see whether 1 exists in the or input of the unit circuit 184 and the OR outputs ultimately indicate under the control of the circuit 184 that any one of the I input signals of the plurality of unit circuits 182 is 1.

Fig. 6(c) shows another unit circuit 186 in the high tier with the OR output of the circuit 184 as an input and as stated above, the unit circuit 186 can be exactly the same in structure as the unit circuits 182 and 184 respectively shown in Figs. 6(a) and 6(b). The unit circuit 186 shown in Fig. 6(c) uses the OR outputs of all the four unit circuits 184 forming the intermediate tier as OR inputs OR_k (k = 0, 1, 2, 3) and outputs OUT_0, OUT_1, OUT_2, OUT_3 corresponding to the OR inputs OR_k (k = 0, 1, 2, 3) are applied to respective enable signal inputs E as respective enable signals of all the four unit circuits 184 in the intermediate tier. Therefore, the OR output GOR of the unit circuit 186 may be used to see whether 1 exists in the OR input OR_k of the unit circuit 186. The enable signal ENB of the unit circuit 186 itself is supplied with a predetermined clock signal separately until all of OUT_k output "0", that is, the OR output GOR becomes "0". While the output OUT_k of the unit circuit 186 is outputting "1", the small unit priority circuit having "1" (match signal) conversely exists in a low order group equivalent to the address at which "1" is output as only one signal having "1" (hereinafter called "priority-ordered output signal") selected from among the input signals of the priority circuit 180 has not yet been output completely.

The arrangement of the circuit for effecting hierarchical priority selection by employing the small unit priority circuits 182, 184 and 186 contributes to high-speed operation as compared with a case where all N-channel transistors 44 are serially connected in the form of the single-hierarchical priority circuit 20 as shown in Fig. 2. In this case, the signal state (logical value) of the node Q_3 of the lowest-order circuit element 188_3 of the priority circuit 182 shown in Fig. 6 may be used as the or or OR output. What uses the logical value of the node Q_3 like this is extremely advantageous in that no special circuit is required to obtain the OR output. However, the present invention is not limited to this application but may be practiced in such a way as to increase the operating speed by employing an ordinary OR gate to directly obtain the OR output from the input signal.

Even if there exist hit signals having continuous priorities in different small unit priority circuits 182, the high priority hit signal is output as a priority-ordered output signal by using the or and OR outputs. Even though "1" output from the unit circuit 182 in which a hit signal at a low priority word address exits is possible, the output signal in the unit circuit 184 in the high tier is not allowed to become "1" output until the OR output becomes "0". Consequently, the enable signal in the unit circuit 182 will never become "1" (i.e., active) and the unit circuit 182 is not allowed to

output "1". However, the high tier unit circuit 184 outputs "1" when the OR output of the first priority unit circuit 182 becomes 0 since the OR output of the second priority unit circuit 182 is "1". Therefore, the enable signal in the second priority unit circuit 182 becomes "1" and this unit circuit 182 can output "1". In this way, quick switching is possible even when a hit signal exists between different unit circuits 182.

As the priority circuit 180 of Fig. 5 has 64 inputs, 6 bits and consequently six address lines are needed for address code conversion. When the conventional encode circuit 22 of Fig. 2 is used as an address encoder, a 6-bit address encoder may be formed by connecting the six address lines and the respective four output lines of 16 priority circuits 182 in the lowest hierarchical tier, that is, 64 output lines in total via grounded transistors 52 in the aforementioned predetermined method. Although the priority circuit 180 of Fig. 5 is applicable to the conventional encode circuit, the number of transistors for connecting the output lines and the address lines increases as the number of inputs increases.

The encode circuit 190 of Fig. 5 has an address encoder for encoding two bits in each hierarchical tier of the aforementioned priority circuit 180 of tertiary structure. A priority-ordered output signal is then output when a match signal (hit signal) is contained. However, there exists one output terminal for outputting "1" H (high) in each hierarchical tier out of those forming small unit priority circuits 182, 184, 186 of the priority circuit 180. Therefore, sixteen small unit priority circuits 16 in the lowest tier are connected to two address lines 192_1, 192_0 for determining A_1, A_0 of low order two bits. Four of the priority circuits 184 in the intermediate tier are connected to two address lines 192_3, 192_2 for determining A_3, A_2 of intermediate two bits. One priority circuit 186 in the highest tier is connected to two address lines 192_5, 192_4 for determining A_5, A_4 of high order two bits.

As one priority circuit and two address lines are connected in the same manner in each hierarchical tier, the connection between the lowest tier priority circuit 182_0 and the address lines 192_1, 192_0 will subsequently be described as a representative example. The first output line O_0 of the priority circuit 182_0 is connected to the gate electrodes of two transistors 52 for respectively grounding (or fixing to "0" potential) the address lines 192_1, 192_0. When only the output of the first output line O_0 is "1" [$(O_0, O_1, O_2, O_3) = (1, 0, 0, 0)$], the two grounded transistors 52 are turned on, which results in $A_0 = A_1 = 0$. Then the second output line O_1 of the priority circuit 182_0 is connected to the gate electrode of the grounded transistor 52 for grounding (or fixing to "0" potential) the address line 192_1. Consequently, the transistor 52 is turned on when only the second output line O_1 is "1" [$(O_0, O_1, O_2, O_3) = (0, 1, 0, 0)$], which results in $(A_1, A_0) = (0, 1)$. Further, the third output line O_2 of the priority circuit 182_0 is connected to the gate electrode of the transistor 52 for grounding (or fixing to "0" potential) the address line 192_0. Consequently, the grounded transistor 52 is turned on when only the third output line O_2 is "1" [$(O_0, O_1, O_2, O_3) = (0, 0, 1, 0)$], which results in $(A_1, A_0) = (1, 0)$. In this case, $(A_1, A_0) = (1, 1)$ when only the fourth output line O_3 is "1" [$(O_0, O_1, O_2, O_3) = (0, 0, 0, 1)$].

The address encoder 190 can be fabricated by carrying out the above-noted connections with the two address lines tier-to-tier in each priority circuit. Since the number of transistors used to connect the address lines 192_0 - 192_5 and the respective priority circuits 182, 184, 186 in this address encoder 190 is four per priority circuit, there are 84 transistors in total, namely 64 in the lowest tier, 16 in the intermediate tier and four in the highest tier. On the contrary, 192 transistors are needed in the case of an address encoder of Fig. 2 in which all of six address lines are connected to 16 priority circuits 20 in the lowest tier. Consequently, the encode circuit 190 of Fig. 5 has the effect of high encoding speed.

A description has been given, by way of example, of an arrangement of N-channel transistors connected serially as priority circuits constituting the main encoder and the subblock encoder of the encoder as shown in Figs. 2 and 6(a) according to the present invention. However, the present invention is not limited to such an arrangement but includes using a priority circuit formed of serially-connected P-channel transistors, arranging to make bidirectional priority possible, and utilizing any known main encoder or subblock encoder on condition that a prefetch circuit is provided for the main encoder.

Although encoders in various aspects of the present invention has been described, the present invention is not restricted to these aspects but may needless to say be modified in design and improved in numerous ways in connection with the number of inputs and arrangements of prefetch circuits, data latch circuits, priority circuits and encode circuits constituting the main encoder and the subblock encoder without departing the spirit and scope of the present invention.

As set forth above in detail, when the match retrieval data in the CAM memory block is obtained by means of the encoder according to the present invention, the result of match retrieval in the first CAM subblock among the plurality of CAM subblocks constituting the CAM block, for example, a match signal (hit signal) matching the retrieval data in the plurality of CAM words is held in the holding means such as a register and the block hit signal indicating the presence of the CAM word matching the retrieval data is generated in the CAM subblock. On receiving a block hit signal, the priority subblock encoder subsequently selects the first priority CAM subblock and generates a subblock address. The hit signal (simultaneously

over the whole word) in the first priority subblock thus selected is transferred to the priority encoder. Then the priority encoder encodes the hit signal in the order of predetermined priorities and outputs a word address. The priority subblock encoder selects the second priority CAM subblock during the encoding operation above and applies the hit signal data held in the holding means such as the register of the subblock to the prefetch circuit provided in the main priority encoder. Accordingly, the main priority encoder starts encoding the hit signal data in the second priority subblock stored in the prefetch circuit immediately after the hit signal has been encoded completely and outputs the word address. Then the encoder combines the word address output with the subblock address output and outputs a logical address.

In this aspect of the present invention, output signals from a number of CAM subblocks can be encoded efficiently without delay (switch time) at the time of subblock-to-subblock switching even when the plurality of subblocks constitute a CAM block. As a result, the encoder according to the present invention is applicable to a content addressable bulk memory which has the CAM block comprising the plurality of CAM subblocks and is required to process mass data at high speed.

Referring to Figs. 8 - 11, an encoder in the second aspect of the present invention and a semiconductor integrated circuit in the fourth aspect thereof will be described in detail. The semiconductor integrated circuit in the fourth aspect is a number detection circuit applicable to the encoder in the second aspect.

The encoder in the second aspect of the present invention carries out match retrieval when retrieval data are fed to CAM blocks forming CAM before being transferred to a plurality of CAM subblocks. At this time, the result, that is, flag data including a signal (hit signal) matching the retrieval data is held in the plurality of CAM words on a CAM subblock basis. Then the highest priority CAM subblock is selected by a priority subblock encoder and its flag data is transferred to and held in the flag register of a priority main encoder. The priority main encoder encodes the hit signal in the flag data stored in the flag register in the order of predetermined priorities and outputs a hit address. While the flag data is being encoded, on the other hand, the flag data in the second priority CAM subblock selected by the priority subblock encoder is fed to a prefetch circuit. Hit signals in the flag data in the first priority CAM subblock are sequentially encoded in the priority main encoder and as hit addresses are output, the hit signals in the flag register are sequentially reset.

At this time, a timing detection control circuit means for predetecting the end of the hit signal in the flag register detects the number of hit signals held in the flag register. When the number of remaining hit signals ultimately comes up to one, for example, flag data in the second priority CAM subblock that has been fed to the prefetch circuit is transferred to the flag register immediately after the termination of encoding the preceding hit signal and it is started to encode the hit signal in this flag data. Then flag data in the next priority CAM subblock is prefetched to the prefetch circuit caused to have a free space. These steps are sequentially repeated to encode the hit signals in the whole CAM block, that is, output addresses.

With the encoder according to the present invention, the hit signal of the flag data in the CAM subblock subject to subsequent encoding has been applied to the prefetch circuit while the hit signal in the flag data in the preceding CAM subblock is being encoded, whereby the time required to transfer the hit signal from the CAM subblock to the flag register of the priority main encoder can be saved. It is simultaneously detected that the number of hit signals ultimately becomes one immediately after the encoding of the last hit signal of the flag data in the flag register is started. In the next encoding cycle, the flag data held in the prefetch circuit is transferred to the flag register and the hit signal in the flag data thus transferred is encoded. Since no loss is caused in the encoding cycle, the encoding time in not only the whole CAM block but also the whole CAM can be shortened, so that the high-speed match retrieval operation of CAM becomes possible.

Fig. 8 is a schematic diagram of a CAM block to which the encoder in the second aspect of the present invention is applied.

An encoder 11 of Fig. 8 has a timing control circuit 60 as the semiconductor integrated circuit in a main encoder 12 of the fourth aspect of the present invention and as it is basically similar in structure to the encoder shown in Fig. 1 except that the output of the timing control circuit is used to set the initial value of the flag register (data latch circuit) 18, like component elements are designated by like reference characters and the detailed description thereof will be omitted.

The encoder 11 of Fig. 8 according to the present invention comprises a priority encoder with a prefetch circuit (hereinafter called "main priority encoder" or "main encoder") 12, and a priority subblock encoder (hereinafter called "subblock priority encoder" or "subblock encoder") 14. The main encoder 12 comprises a prefetch circuit 16, a flag register circuit 18, a priority circuit 20, an encode circuit 22, and a timing control circuit 60. The subblock encoder 14 comprises a latch circuit 24, a priority circuit 26, and an encode circuit 28.

Fig. 9 is a block diagram of the main encoder 12 in this aspect of the present invention. In Fig. 9, the prefetch circuit 16 of the main encoder 12 stores the flag data held in the register 36 of the second priority subblock 32 on a word 34 basis (W_0, W_1,..., W_m) while the priority circuit 20 and the encoder circuit 22 of the

main encoder 12 are encoding the hit signal in the flag data in the first priority subblock 32 and the address of the match word 34 in the order of predetermined priorities. In this case, the prefetch circuit 16 may be any apparatus such as a data latch circuit or a data register as long as it is capable of temporarily holding m+1 of 1-bit data "0" or "1". The flag data from the prefetch circuit 16 is fed by the switch timing output (detection output) of the timing control circuit 60 in parallel to the flag register 18. Moreover, the prefetch circuit 16 fetches the flag data in the second priority subblock 32 selected by the subblock encoder 14 per each word 34 while the flag data is being encoded by the main encoder 12.

More specifically, the timing control circuit 60 in the main encoder 12 as shown in Fig. 9 detects the number of flag data (high signals), for example, the last one held in the flag register 18, applies a switch timing signal (initial value setting signal) to the flag register 18 and feeds the flag data in the prefetch circuit 16 to the flag register 18. After the last hit signal in the flag data held in the flag register 18 is reset in the case of the main encoder 12 in the first aspect of Fig. 2, termination data "0" as an OR output from the Q_m node of the priority circuit 20 is used to switch the flag data in the flag register 18 over to flag data in the second priority subblock latch-held in the prefetch circuit 16. In other words, OR output "0" of node Q_m is output from the OR output terminal $\overline{or}$ and inverted by the inverter 49, the inverted value "1" being supplied to the flag register 18. The flag data of the following priority subblock 32 latch-held in the prefetch circuit 16 is fed to (shifted in) the corresponding circuit of the flag register circuit 18 and held therein. Then the flag data in the subsequent priority subblock 32 selected by the subblock encoder 14 beforehand is read from and latch- held in the register 36 to a vacant prefetch circuit in this aspect of the present invention as well as the first one. The priority circuit 20 thus terminates the processing of the flag data in the first priority subblock and since it need not wait for the flag data in the second priority subblock transferred from the register 36 of the subblock 32, it can perform the encoding operation with efficiency likewise according to the method in the first aspect of the present invention. In the first aspect, however, there occurs a cycle in which the flag data in the subblock is impossible to encode when it is switched in the priority encode cycle started by resetting since the contents of the flag register 18 are switched over to the second priority flag data held in the prefetch circuit after the last hit signal in the flag data in the first priority subblock held in the flag register is reset. As a result, there is produced a time during which no encode output operation can be performed.

In the first aspect of the present invention, instead of resetting the last hit signal in the prefetch circuit 20 with the result of detection as an input signal when the last hit signal is detected after the number of hit signals in the flag data in the flag register 18 is detected by means of the timing control circuit 60 to be described below, the flag data in the second priority subblock 32 held in the prefetch circuit 16 is shifted (input) to the flag register 18. With respect to even the flag data in the identical subblock, priority encoding can be carried out in the same cycle even when the flag data in the subblock is varied. Needless to say, the prefetching time (the time required to transfer the flag data from each subblock 32 to the main encoder 12) is made irrelevant to the encoding process by prefetching the flag data in the third priority subblock 32 preselected by the subblock encoder 14 from the register 36 to the prefetch circuit 16 caused to have a free space by switching the flag data in the subblock of the flag register 18 according to the present invention and latch-holding the result. Encoding efficiency can thus be improved. Moreover, the last hit signal in the flag data in the flag register 18 need not be reset.

Fig. 10 is a circuit diagram of a specific timing control circuit 60 to which the semiconductor integrated circuit in the fourth aspect of the present invention is applied, the semiconductor integrated circuit featuring the encoder 11 in the second aspect of the present invention in the best way.

The timing control circuit 60 of Fig. 10 according to the present invention comprises a first signal line (signal current detection line) 62, a second signal line (reference current drive line) 64, m+1 of current drive circuits (current drive means) 66_0, 66_1,..., 66_m provided for respective m+1 of data latch circuits 18_0, 18_1,..., 18_m of a flag register 18 in parallel to the first signal line 62, a reference current drive circuit (reference current drive means) provided for the second signal line 64, a differential current detection circuit (differential current detection means) 70 for detecting the difference between the currents flowing through the first and second signal lines 62, 64, that is, detecting the differential current, and a precharge control signal line 72 for controlling the operation timing of the timing control circuit, namely, the current drive circuits 66 (66_0, 66_1,..., 66_m), the reference current drive circuit 68 and the differential current detection circuit 70.

In the timing control circuit 60 according to the present invention, dummy circuits 74 (74_0, 74_1,..., 74_m) are provided for the second signal line 64 as those correspond to the current drive circuits 66 (66_0, 66_1,..., 66_m) provided for the first signal line 62, whereas a dummy circuit 76 is provided for the first signal line 62 as what corresponds to the reference current drive circuit 68 provided for the second signal line 64. Moreover, one ends of both the first and second signal lines 62, 64 are connected to the differential detection circuit 70. Respective precharge transistors 78 and a transistor 79 for keeping at the same po-

tential are also connected to the signal lines 62 and 64. These transistors 78 and 79 function to initialize both signal lines 62 and 64 to a predetermined potential, for example, 5V. In this case, the transistors 78, 79 are formed with P-channel MOS transistors and their gate electrodes are connected to the precharge control signal line 72. Moreover, one of the dummy circuits 74 (74_0, 74_1,..., 74_m) may be made the reference current drive circuit 68. Then the dummy circuit 76 can be dispensed with.

One of the current drive circuits 66 will be described as what represents them. The current drive circuit 66 comprises a control transistor 67a and a signal voltage application transistor 67b which are formed with two N-channel MOS transistors connected in series. The transistor 67a is connected to the first signal line 62, whereas the transistor 67b is grounded. The gate electrode of the transistor 67a is connected to the control signal line 72 and the gate electrode of the transistor 67b to the output terminal Q of the corresponding data latch circuit of the flag register 18.

The transistor 67a of the current drive circuit 66 is held ON at the time of detection and when a hit signal "1" is applied from the flag register 18 to the gate electrode of the transistor 67b, the transistor is turned on and causes a predetermined current i_0 to flow. The drive current i_0 is arranged so as to make it has the same intensity in all of the current drive circuits 66_0, 66_1,..., 66_m, though it slightly varies to an extent resulting from the variations of the transistors 67a, 67b for use, for example, variation in process. The dummy circuit 74 is also similar in structure to the current drive circuit 66 and comprises two N-channel MOS transistors 75a, 75b with one end connected to the second signal line 64, the other being grounded. The gate electrode of the transistor 75a is connected to the control signal line 72 likewise, whereas the gate electrode of the transistor 75b is grounded so that it is not allowed to be turned on at all times.

On the contrary, the reference current drive circuit 68 is used for causing a predetermined reference current i_r to flow through the second signal line 64 and provided with two N-channel transistors 69a, 69b connected in series. The transistor 69a is connected to the second signal line 64 and its gate electrode to the control signal line 72. The transistor 69b is grounded and its gate electrode is connected to the power supply at H (high) potential so that it is held ON at all times. On the other hand, the dummy circuit 76 comprises N-channel MOS transistors 76a, 76b similar in structure to those in the dummy circuit 74 except that it is connected to the first signal line 62. The reference current value i_r may properly be determined according to the value i_0 of the current that can be made to flow by the current drive circuit 66 (66_0, 66_1,..., 66_m) and the number of hit signals to be detected, and may be greater than i_0 but less than $2i_0$ and the value at which the differential current detection circuit 70 to be described below is able to detect the differential current in order for the last one of the hit signal to be detected. The current value i_r may be determined in consideration of the variations of the circuit elements such as the component transistors 67a, 67b, 69a, 69b, and may preferably be $i_r = 1.2i_0 - 1.8i_0$, for instance.

The differential current detection circuit 70 detects the intensity of the current flowing down both signal lines 62 and 64 and is a current drive type latch circuit for latch-holding the great side of the flowing current at L (low) and the small side thereof at H (high). The differential current detection circuit 70 comprises P-channel MOS transistors (PMOSs) 80a, 80b connected to the power supply at the same potential as the potential at the other ends of both signal lines 62 and 64, for example, 5V, N-channel MOS transistors (NMOS) 82a, 82b connected to the above-noted transistors in series, and two precharge transistors 83 as PMOSs. The gate electrodes of the transistors 82a and 80a connected to the first signal line 62 are connected to each other and also to the contact B between the transistors 80b and 82b. Moreover, the gate electrodes of the transistors 82b and 80b connected to the second signal line 64 are connected to each other and also to the contact A between the transistors 80a and 82a. An output line extends from the contact B and is connected via an inverter 84 to an output terminal 85.

Subsequently, the detecting operation of the timing control circuit 60 will be described as a representative example in a case where the last one of the hit signal of the flag data in the flag register 18, that is, the last hit signal is detected. In this case, flag data having a plurality of hit signals ("1") is held in the flag register 18 on the assumption that the reference current i_r is 1.5 times as great as the drive current i_0 of one current drive circuit 66, that is, set at 1.5 i_0.

With the precharge control signal line 72 at L (low: "0"), both precharge transistors 78 and the transistor 79 are first turned on to precharge the first and second signal lines 62 and 64, consequently contacts a and b at H (high) potential (e.g., 5V). Further, both precharge transistors 83 and the transistors 80a, 80b are turned on to precharge the contacts A and B within the differential current detection circuit 70 at H (high) potential (e.g., 5V) likewise. Incidentally, the transistors 82a, 82b of the differential current detection circuit 70, the transistors 67a of all current drive circuits 66 and the transistor 68a of the reference current drive circuit 68 are held off.

With the precharge control signal line 72 at H (high: "1"), the PMOS transistors 78, 79, 80a, 80b, 83 are subsequently turned off, whereas the NMOS transistors 67a, 69a, 75a, 77a are turned on. Both the two transistors 69a, 69b of the reference current drive circuit 68 are turned on accordingly and the reference current i_r (= 1.5 i_0) flows through the second signal

line 64 to lower the potential of the contact b. On the other hand, the transistor 67b having the gate electrode connected to the data latch circuit 18j of the flag register 18 whose flag data has the hit signal "1" out of m+1 of current drive circuits 66 (66_0, 66_0,..., 66_m) is turned on and the transistor 67a is held on, whereby the drive current i_0 flows from the first signal line 62 through the current drive circuit 66j. Since the flag data in the flag register 18 has a plurality of hit signals "1", for example, k ($k \geqq 2$) of hit signals in this case, current of ki_0 flows through the first signal line 62 and the potential of the contact a drops accordingly.

When k is greater than 2, the potential of the contact a drops faster than that of the contact b because current ki_0 flowing through the first signal line 62 is greater than the reference current i_r (= 1.5 i_0) flowing through the second signal line 64. When the difference between the gate potential (potential at the contact B) of NMOS 82a and the source potential (potential of the contact a) becomes greater than the substrate-biased threshold voltage (e.g., 1.4V) of NMOS 82a, that is, the potential of the contact a becomes lower than 3.6V, NMOS 82a is turned on and the potential of the contact A drops. However, the potential of the contact b has not yet so much lowered as to turn on NMOS 82a, which remains in the off state accordingly. Although the current flows through both signal lines 62 and 64 then to cause the potential at the contacts A and a to drop further, NMOS 82b keeps the off state as the potential drop at the contact A is greater than the potential drop at the contact b. The contact A thus turns to "0". On the other hand, the contact B remains at "1" and the output of the inverter 84 keeps "1"..

As the plurality of hit signals "1" within the flag register 18 are encoded, they are reset to "0" one after another. When the number of remaining hit signals comes up to one, the timing control circuit 60 performs the detecting operations, that is, first precharges the precharge control signal line 72 by applying "0" and then applying "1" thereto, thus causing the current i_0 and the reference current i_r (= 1.5 i_0) to flow through the first and second signal lines 62, 64 likewise, respectively. Since the current flowing through the second signal line 64 is greater at this time, the potential of the contact b drops faster than that of the contact a and NMOS 82a conversely keeps the off state, whereas NMOS 82b is held ON. Consequently, the potential of the contact B drops, and the signal thereat is inverted by the inverter 84, whereby "1" is output from the output terminal 85.

Further, it is significantly important that both signal lines 62 and 64 being precharged beforehand at the supply potential (e.g. 5V) in order to obtain stable operation of the differential current detection circuit 70. That is, since a time margin is available before the charge of either signal line 62 or 64 drops to the operation potential 3.6V of the differential current detection circuit 70, the latch type differential current detection circuit can have a spare time for the operation timing which enables elimination of such effects as switching noises of control line.

As a result, it is apparent that more than one hit signal "1" is held in the flag register 18 if the output signal from the output terminal 85 of the timing control circuit 60 is "0" and the number of hit signals is one or less if the output signal is "1". When the output signal is changed from "0" to "1", the result of detection, for example, the "1" signal or the signal change may be used to switch the flag data in the flag register 18 over to what is in the prefetch circuit 16. Needless to say, the output signal may be fetched from the contact A.

Fig. 11 shows an encode time chart using the timing control circuit 60.

In Fig. 11, (a) represents an encode timing in the main encoder 12; (b) a reset timing of the hit signal "1" in the flag register 18; (c) detection timing in the timing control circuit 60; (d) variation of the output signal of the timing control circuit 60; and (e) timing at which the flag data in the prefetch circuit 16 is shifted to the flag register 18.

While the hit signal in the same flag data held in the flag register 18 is being encoded with the predetermined priority, it has been so arranged that the encode cycle is started (rise) after a passage of fixed time followed from the rise timing of the reset pulse of the hit signal. When, however, the timing control circuit 60 detects the last hit signal at the detection timing activated by the encode pulse, with the output signal (d) changed from "0" to "1", a pulse circuit 87 of Fig. 10 generates pulse for alternatively feeding the flag data in the prefetch circuit 16 to the flag register 18 with the timing at which the reset pulse should have been generated so as to switch the flag data in the flag register 18. Moreover, the flag data is used to make the priority circuit 20 and the encode circuit 22 perform the encode operation in the continuous encode cycle to output an encode address. The main encoder 12 thus performs the encode operation in the predetermined continuous cycle and produces an encode output. The main encoder 12 is basically arranged as stated above.

As previously noted, the encoder according to the second aspect of the present invention has the effect, in addition to what has been achieved in the aforementioned first aspect, of starting the encoding of the flag signal data in the second priority subblock that has previously been fed to the prefetch circuit in the continuous cycle after the priority encoder terminates the encoding the hit signal by means of a data switch timing control circuit, encoding the data and outputting a word address.

With the encoder in this aspect of the present invention, the memory block, though it is provided with the plurality of CAM subblocks, can encode output

signals from a number of CAM subblocks efficiently in the continuous cycle without subblock-to-subblock switch delay (switch time). Consequently, this encoder is applicable to a content addressable bulk memory which has the CAM block comprising the plurality of CAM subblocks and is required to process mass data at high speed.

With the semiconductor integrated circuit in the fourth aspect of the present invention, it is possible to detect accurately and quickly the fact that the number of data "0" or "1" fed to the current drive means has reached a preset value.

Referring to Figs. 12 - 14, a semiconductor integrated circuit in the fifth aspect of the present invention will be described in detail.

This aspect of the present invention is applicable to the encoder in the second aspect thereof as a number detection circuit for timing control.

In the semiconductor integrated circuit in this aspect of the present invention, there is preset the reference current i_r made to flow in the reference current drive means provided on the reference current drive line as the second signal line in accordance with the number of data k_0 ($M > k_0 \geqq 0$) desired to be detected out of the data "1" or "0" fed to data input lines for respectively controlling M ($M \geqq 1$) provided in parallel on the first signal line, or the signal current detection line, that is, a current value ($k_0 i_0 < i_r < (k_0 + 1) i_0$) greater by k_0 times and smaller by $k_0 + 1$ times than the current value i_0 flowing through one current drive means. Each current drive means of the semiconductor integrated circuit has a signal voltage application transistor whose gate electrode is connected to the data input line and a control transistor for controlling the operating time of the semiconductor integrated circuit, the signal voltage application transistor being provided on the signal current detection line side.

Therefore, the operating timing is set in the semiconductor integrated circuit in this aspect of the present invention and the control transistors of the whole current drive means as well as those of the reference current drive means are controlled. When these transistors are turned on, the current flows through the current drive means as all the signal voltage application transistors of the current drive means with the data input line supplied with desired data, whereby current i ($i = ki_0$) in proportion to the number k ($M > k \geqq 0$) flows through the signal current detection line. On the other hand, the reference current value i_r is caused by the reference current drive means to flow through the reference current drive line. The differential current detection means detects the differential current between the values i and i_r of the current flowing through both the signal lines and outputs the inversion of the differential current, that is, the inverted (timing) with respect to the size relation between both the current value i and i_r. It is thus detected that the number k of desired data out of those fed to the respective input lines has reached the preset value k_0. The semiconductor integrated circuit according to the present invention is capable of detecting the number of desired data fed to the data input lines.

With the control transistor of the current drive means provided closer to the current signal detection line than the signal voltage application transistor, the semiconductor integrated circuit is set at the operating timing even though the data fed to the data input line is not what has been desired while the signal voltage application transistor is held OFF. Since current temporarily flows from the signal current detection line to the control transistor, the current also flows into the signal current detection line at the time the operation is started. The difference between the current flowing through the detection line when the detection is required and what flows through the reference current drive line decreases accordingly and this makes it difficult to detect the inversion of the differential current by means of the differential current detection means. No accurate detecting operation may be performed stably in that case because of noise.

Since the signal voltage application transistor is provided closer to the signal current detection line than the control transistor in the semiconductor integrated circuit, the current will not flow from the signal current detection line unless the signal voltage application transistor is turned on even if the control transistors of the whole current drive means are turned on. Therefore, the differential current between the current flowing through the signal current detection line and the reference current because of the voltage application transistor that has been turned on can be detected clearly to a degree even when the detection thereof is needed. As a result, the inversion of the differential current can be detected by the differential current detection means quickly and stably with accuracy.

Fig. 12 shows a specific circuit diagram of a timing control circuit 61 to which the semiconductor integrated circuit in the fifth aspect of the present invention is applied. The timing control circuit 61 of Fig. 12 is applied to the encoder 11 in the second aspect of the present invention shown in Fig. 8 and as it is exactly the same in structure as the timing control circuit 60 of Fig. 10 except for the configuration of the signal voltage application transistor 67c and the control transistor 67d of the current drive circuit 66, and that of the transistors 69c and 69d of the reference current drive circuit 68, like component elements are designated by like reference characters and the detailed description thereof will be omitted.

One of the current drive circuits 66 which best features the timing control circuit of Fig. 12 will be described as what represents them. The current drive circuit 66 comprises a signal voltage application transistor 67c and a control transistor 67d which are

formed with two N-channel MOS transistors connected in series. The signal voltage application transistor 67c is connected to the first signal line 62, whereas the control transistor 67d is grounded. The gate electrode of the signal voltage application transistor 67c is connected to the output terminal Q of the corresponding data latch circuit of the flag register 18 and the gate electrode of the transistor 67d to the control signal line 72.

The control transistor 67d of the current drive circuit 66 is held ON at the time of detection and when a hit signal "1" is applied from the flag register 18 to the gate electrode of the signal voltage application transistor 67c, the signal voltage application transistor 67c is turned on and causes a predetermined current i_0 to flow. The drive current i_0 is arranged so as to make it has the same intensity in all of the current drive circuits 66_0, 66_1,..., 66_m, though it slightly varies to an extent resulting from the variations of the transistors 67a, 67b for use, for example, variation in process. The dummy circuit 74 is also similar in structure to the current drive circuit 66 and comprises two N-channel MOS transistors 75c, 75d with one end connected to the second signal line 64, the other being grounded. The gate electrode of the grounded transistor 75d is connected to the control signal line 72 likewise, whereas the gate electrode of the transistor 75c on the side of the second signal line 64 is grounded so that it is not allowed to be turned on at all times.

On the contrary, the reference current drive circuit 68 is used for causing the predetermined reference current i_r to flow through the second signal line and provided with two N-channel transistors 69c, 69d connected in series. The transistor 69c is connected to the second signal line and its gate electrode to the power supply at H (high) potential so that it is held ON at all times. The transistor 69d is grounded and its gate electrode is connected to the control signal line 72. Moreover, the dummy circuit 76 of the reference current drive circuit 68 is connected to the first signal line 62. The reference current value i_r may properly be determined according to the value i_0 of the current that can be made to flow by the current drive circuit 66 (66_0, 66_1,..., 66_m) and the number of hit signals to be detected, and may be greater than i_0 but less than $2i_0$ and the value at which the differential current detection circuit 70 to be described below is able to detect the differential current in order for the last one of the hit signal to be detected. The current value i_r may be determined in consideration of the variations of the circuit elements such as the component transistors 67c, 67d, 69c, 69d, and may preferably be $i_r = 1.2i_0 - 1.8i_0$, for instance.

An output line is extended from the contact B of the differential detection circuit 70 and connected via an inverter 84 to an AND circuit 88. The reset signal of the flag register 18 is applied to one input of the AND circuit 88. The output of the AND circuit 88 is connected to the clock terminal of the flag register 18.

Subsequently, the detecting operation of the timing control circuit 61 will be described as a representative example in a case where the last one of the hit signal of the flag data in the flag register 18, that is, its last hit signal is detected. In this case, flag data having a plurality of hit signals ("1") is held in the flag register 18 on the assumption that the reference current i_r is 1.5 times as great as the drive current i_0 of one current drive circuit 66, that is, set at 1.5 i_0.

With the precharge control signal line 72 at L (low:"0"), both precharge transistors 78 and the transistor 79 are first turned on to precharge the first and second signal lines 62 and 64, consequently contacts (nodes) a and b at H (high) potential (e.g., 5V). Further, both precharge transistors 83 are turned on to precharge the contacts A and B within the differential current detection circuit 70 at H (high) potential (e.g., 5V) likewise. Incidentally, the transistors 82a, 82b of the differential current detection circuit 70, the transistors 67d of the whole current drive circuit 66 and the transistor 69d of the reference current drive circuit 68 are held off.

With the precharge control signal line 72 at H (high: "1"), the PMOS transistors 78, 79, 83 are subsequently turned off, whereas the NMOS transistors 67d, 69d, 75d, 77d are turned on. Both the two transistors 69c, 69d of the reference current drive circuit 68 are turned on accordingly and the reference current i_r (= 1.5 i_0) flows through the second signal line 64 to lower the potential of the contact b. On the other hand, the transistor 67c having the gate electrode connected to the data latch circuit 18j of the flag register 18 whose flag data has the hit signal "1" out of m+1 of current drive circuits 66 (66_0, 66_0,..., 66_m) is turned on and the control transistor 67d is held on, whereby the drive current i_0 flows from the first signal line 62 through the current drive circuit 66j. Since the flag data in the flag register 18 has a plurality of hit signals "1", for example, k ($k \geqq 2$) of hit signals in this case, current of ki_0 flows through the first signal line 62 and the potential of the contact a drops accordingly.

When k is greater than 2, the potential of the contact a drops faster than that of the contact b because current ki_0 flowing through the first signal line 62 is greater than the reference current i_r (= 1.5 i_0) flowing through the second signal line 64. When the difference between the gate potential (potential at the contact B) of NMOS 82a and the source potential (potential of the contact a) becomes greater than the substrate-biased threshold voltage (e.g., 1.4V) of NMOS 82a (for example, the potential of the contact a drops up to 3.6V when the potential of the contact B is 5V), NMOS 82a is turned on and the potential of the contact A drops. However, the potential of the contact b has not yet so much lowered as to turn on NMOS 82b, which remains in the off state accordingly. Although

the current flows through both signal lines 62 and 64 then to cause the potential at the contacts A and a to drop further, NMOS 82b keeps the off state as the potential drop at the contact a, that is, at the contact A is greater than the potential drop at the contact b. The contact B thus keeps "1" and "0" is applied by the inverter 84 connected thereto to the AND circuit 88. On the other hand, the contact A remains at "0".

As the plurality of hit signals "1" within the flag register 18 are encoded, they are reset to "0" one after another. When the number of remaining hit signals comes up to one, the timing control circuit 60 according to the present invention performs the detecting operation, that is, first precharges the precharge control signal line 72 by applying "0" and then applying "1" thereto, thus causing the current i_0 and the reference current i_r (= 1.5 i_0) to flow through the first and second signal lines 62, 64 likewise, respectively. Since the current flowing through the second signal line 64 is greater at this time, the potential of the contact b drops faster than that of the contact a and NMOS 82a conversely keeps the off state, whereas NMOS 82b is held ON. Consequently, the potential of the contact B drops to the low level and inverted by the inverter 84 so that "1" is applied to the AND circuit 88. The potential of the contact A is maintained at H (high) potential.

As a result, it is apparent that more than one hit signal "1" is held in the flag register 18 if the output signal from the inverter 84 of the timing control circuit 61 in this aspect of the present invention is "0" and the number of hit signals is one or less if the output signal is "1". When the output signal is changed from "0" to "1", the result of detection, that is, a switch control signal is obtainable from the "1" signal and the reset signal of the flag register 18 by means of the AND circuit 88. Further, this switch control signal may be used to switch the flag data in the flag register 18 over to the flag data in the prefetch circuit 16. Needless to say, the output signal may be fetched from only the contact A or both contacts A and B.

As previously noted, the timing control circuit 60 of Fig. 10 is exactly the same as the timing control circuit 61 of Fig. 12 except for the reversed arrangement of the control transistor 67a and the signal voltage application transistor 67b in the current drive circuit 66 (66_0, 66_1,..., 66_m) and that of the control transistor 75a and the gate-grounded transistor 75b in the dummy circuit 74 (74_0, 74_1,..., 74_m). It is thus detectable when the number of hit signals applied to the gate electrode of the signal voltage application transistor 67b and held by the data latch circuit of the flag register 18 has reached the predetermined value, for example, ultimately one.

When the timing detecting operation is started in both timing control circuits 60 and 61, the current corresponding to the number of hit signals ("1") in the flag register 18 flows into the signal current detection line (the first signal line) 62 and the predetermined reference current into the reference current drive line (the second signal line) 64. Therefore, the differential current detection circuit 70 detects the small potential difference between the contacts a, b resulting from the difference between the currents flowing through both signal lines 62 and 64 as a great potential difference at the contacts A, B one side of which (high potential sides of the contacts a, b) is held at the precharge voltage (e.g., V_{dd}), the other side (low potential sides thereof) being lowered up to the ground level (e.g., 0V).

The subsequent changes of the contacts A and B precharged at the same potential (e.g., V_{dd} = 5V) are determined by which one of the transistors 82a and 82b is turned on. In other words, the current flows through the first and second signal lines 62 and 64 during the operation of timing detection, thus causing the potentials of the contacts a and b of both signal lines 62, 64 to drop as previously noted. When either one of the potential difference between the contacts B and a and the potential difference between the contacts A and b exceeds the substrate-biased threshold value (e.g., 1.4V), that is, when either one of the potentials of both signal lines 62 and 64 (those of the contacts a and b) drops beyond the threshold value (e.g., 1.4V)(to lower than 3.6V), one of the transistors 82a and 82b is turned on. As a result, the contact A or B on the side of the energized transistor 82a or 82b immediately becomes equal in potential to the contact a or b thus lowered and lowers up to the ground level (0V) together. On the other hand, the contact A or B on the side of the de-energized transistor 82a or 82b is maintained at the precharged potential (5V).

It is thus possible to detect the predetermined number of hit signals (e.g., ultimately only one) by making the potential of the contact B a detection signal and by taking out the output signal via the inverter 84. In other words, the transistor 82b is turned on as the inverter 84 has been connected to the tip of the contact B and the potential of the contact B then drops. When the potential becomes lower than the threshold value (e.g., about 2.5V) of the inverter 84, the output signal "1" is obtained.

If the potential difference between the contacts a and b is excessively small when the contacts A and B branch off in the differential current detection circuit 70, the ON-operation of the transistors 82a and 82b becomes irrelevant to the potential difference between the contacts a, b, that is, the possibility of malfunction increases. Therefore, the greater the potential difference between both contacts a and b, the less the transistors may be seriously affected thereby. Stable accurate timing detection is thus always assured. In the timing control circuit 60 of Fig. 10, however, the control transistor 67a of the current drive circuit 66 is connected to the first signal line 62 as the signal current detection line; the other elec-

trode of the signal voltage application transistor 67b connected to the control transistor 67a in series; the control transistor 75a of the dummy circuit 74 is connected to the second signal line as the reference current drive line; and the other electrode of the gate-grounded transistor 75b connected to the control transistor 75a in series is grounded. When the precharge operation of the precharge control signal line 72 at low (L: "0") level is changed to the timing detecting operation at high (H: "1") level, the control transistor 67a of the current drive circuit 66 is turned on, despite the data held in each data latch circuit 18j (j = 0,..., m) of the flag register 18 and there occurs the temporary inflow of charge between the control transistor 67a and the signal voltage application transistor 67b. Likewise, the control transistor 75a of the dummy circuit 74 is turned on and there occurs the temporary inflow of charge between the control transistor 75a and the gate-grounded transistor 75b.

As a result, the current flows from the first and second signal lines 62 and 64 into the current drive circuit 66 and the control transistors 67a and 75a of the dummy circuit 74 in the initial stage of the timing detecting operation as shown in Fig. 14(b) and the potentials of the contacts a and b of the respective signal lines 62, 64 simultaneously drop. If the number of data latch circuits of the flag register 18 and the number of corresponding current drive circuits 66 and dummy circuits 74, the current flowing through the first and second signal lines 62 and 64 increases in the initial stage of detection, thus causing the potentials of the contacts a and b to drop simultaneously and sharply. Consequently, the potential difference between the contacts a and b slowly develops when the signal voltage application transistor 67b is turned on, and the then potentials of both tends to become low; in other words, their potentials lower beyond the predetermined value (e.g., 3.6V) of the potential of either signal line 62 or 64 (either contacts a or b). The potential difference between the contacts a and b becomes small when either transistor 82a or 82b is turned on.

In the timing circuit 61, however, the signal voltage application transistor 67c of the current drive circuit 66 is provided on the side of the first signal line 62 and the control transistor 67d on the grounding side, whereas the gate-grounded transistor 75c of the dummy circuit 74 is connected to the second signal line and the control transistor 75d on the grounding side. Therefore, not only the whole control transistor 67d of the current drive circuit 66 but also the whole control transistor 75d of the dummy circuit 74 is not turned on unless the signal voltage application transistor 67c is turned on even though the timing detecting operation is started. Therefore, no current for charging the control transistors 67d, 75d is allowed to flow through both signal lines 62, 64 in the initial stage of the detecting operation. In consequence, the signal voltage application transistor 67c and the control transistor 67d of every current drive circuit 66 corresponding to the data latch circuit of the flag register 18 holding the hit signal "1" are only turned on; only the current in proportion to the number of them flows through the first signal line 62. Then only the transistors 69c, 69d of the reference current drive circuit 68 are turned on, so that only the reference current flows through the second signal line 64. The potential difference between the contacts a and b is produced immediately after the detecting operation, that is, at a point of time the potential of both contacts a, b slightly drops as shown in Fig. 14(a), whereby the potential difference between both contacts can be secured by a large margin when the potential of either contact a or b drops under the predetermined value (e.g., 3.6V).

In the timing circuits 60 and 61 shown in Figs. 10 and 12, the potential difference between both contacts a and b differs when either contact a or b drops under the predetermined value (e.g., 3.6V). Referring to the examples (a) and (b) shown in Fig. 14 (examples of the timing circuits 61 and 60 of Figs. 12 and 10, respectively), the potential difference between the contacts a and b is about 0.3V in the case of Fig. 14(a), whereas it is about 0.1V in the case of Fig. 14(b), at the point of time the contact b drops under 3.6V at which the contacts A and B start branching off. This means the timing circuit 61 in this aspect of the present invention shown in Fig. 14(a) has a greater noise margin and consequently the differential current detection circuit 70, even if subjected to noise influence, may less malfunction to ensure accurate stable timing detection at all times.

Further, for contacts a and b of Fig. 14, a large potential difference between contact a and b is available at the occasion potential of the contacts a or b drops to 3.6V by precharging both signal lines 62 and 64 beforehand. However, normal operation of the contacts a and b can not be expected due to no potential difference is available in case of both signal lines 62 and 64 are not precharged beforehand. Accordingly, it is important to operate the contacts a and b of Fig. 14 after precharging of the signal lines.

Figs. 14(a) and (b) show detection timing (variation of voltage on the precharge control signal line 72) in the respective timing circuits 61 and 60, with the supply voltage (V_{dd}) at 5V, with the number m+1 of current drive circuits 66 and dummy circuits 74 being 256 and with the reference current i_r being 1.5 i_0; detection timing when the last one of the hit signal "1" is held in the flag register 18; variations of the potentials of the contacts a, b and A, B; and the output signal of the inverter 84.

The timing circuit 61 is basically arranged as stated above.

Fig. 13 is a time chart illustrating encode timing in the main encoder 12 of the encoder 11 of Fig. 8 us-

ing timing circuit 61.

In Fig. 13, (a) represents an encode signal indicating encode timing in the main encoder 12; (b) a reset pulse indicating the reset timing of the hit signal "1" in the flag register 18; (c) a detecting operation signal (voltage applied to the precharge control signal line 72) indicating the detecting operation timing in the timing control circuit 61 according to the present invention; (d) a detection output signal indicating variation of the potential at the contact B of the timing control circuit 61 in this aspect of the present invention; (e) the output signal resulting from inverting the detection output signal of (d) by means of the inverter 84; and (f) a flag data switch control signal showing the timing at which the flag data in the prefetch circuit 16 is shifted to the flag register 18.

While the hit signal in the same flag data held in the flag register 18 is being encoded with the predetermined priority, that is, if the detection output signal (d) is at (H) high level, it has been so arranged that the encode cycle is started (rise) after a passage of fixed time from the rise timing of the reset pulse (d) of the hit signal. When, however, the timing control circuit 60 detects the last hit signal at the detection timing activated by the encode pulse (a), with the detection output signal (d) changed from high (H) level "1" to low (L) level "0", the inverted output signal (e) is changed from "0" to "1". In this case, the AND circuit 88 of Fig. 12 is used for ANDing the inverted output signal (e) of the detection output signal (d) and the reset pulse (b) so as to generate the switch control pulse (f) for alternatively feeding the flag data in the prefetch circuit 16 to the flag register 18. The flag data in the flag register 18 is thus replaced by means of the switch control pulse (f).

As previously noted in detail, the control transistor is not turned on unless the signal voltage application transistor is turned on even at the detection operating timing since the signal voltage application transistor of the current drive means is provided on the signal current detection line side and the control transistor on the grounding side. The charge for charging the whole control transistor is prevented from flowing out of the signal current detection line and this also prevents the differential current detection means from detection failure and malfunction to ensure that the differential current between the reference current drive line and the signal current detection line is detected stably and quickly with accuracy. Therefore, the semiconductor integrated circuit is suitably usable as a timing control circuit for notifying the termination of the encoding operation performed by the CAM encoder.

Referring to Figs. 15 - 17, a semiconductor integrated circuit in the sixth aspect of the present invention will be described in detail. The semiconductor integrated circuit in this aspect of the present invention, like those in the fourth and fifth aspects, is applicable to the encoder in the second aspect thereof as a number detection circuit for timing control.

In the semiconductor integrated circuit in this aspect of the present invention, there is preset the reference current i_r made to flow in the reference current drive means provided on the reference current drive line as the second signal line in accordance with the number of data k_0 ($M > k_0 \geqq 0$) desired to be detected out of the data "1" or "0" fed to data input lines for respectively controlling M ($M \geqq 1$) provided in parallel on the first signal line, or the signal current detection line, that is, a current value ($k_0 \cdot i_0 < i_r < (k_0+1)\, i_0$) greater by k_0 times and smaller by k_0+1 times than the current value i_0 flowing through one current drive means. Each current drive means of the semiconductor integrated circuit has a signal voltage application transistor whose gate electrode is connected to the data input line and a control transistor for controlling the operating time of the semiconductor integrated circuit.

Therefore, the operating timing is set in the semiconductor integrated circuit in this aspect of the present invention and when the whole current drive means with the reference current drive means and the data input line supplied with the desired data is turned on, reference current i_r is caused by the reference current drive means to flow through the reference current drive lines on one hand and current i_0 flows through each current drive means on the other hand. As a result, current i ($i = ki_0$) in proportion to the number k ($M > k \geqq 0$) flows through the signal current detection line. The differential current detection means detects the differential current between the values i and i_r of the current flowing through both the signal lines and outputs the inversion of the differential current, that is, the inverted (timing) with respect to the size relation between both the current value i and i_r. It is thus detected that the number k of desired data out of those fed to the respective input lines has reached the preset value k_0. The semiconductor integrated circuit according to the present invention is capable of detecting the number of desired data fed to the data input lines.

The reference current drive line (reference current line) and the signal current detection line (detection line) have been set at a constant voltage level (V_0). Therefore, the voltage difference between both signal lines, resulting from the current difference between the reference current i_r flowing through the reference current line and the whole signal current i (ki_0) flowing through the detection line when the predetermined time has elapsed after the commencement of the detecting operation, that is, at the time of the predetermined voltage drop from the set voltage level (V_0) or at the raised voltage level, becomes greater than the difference when the detecting operation is started, that is, at the time both signal lines are substantially set at the constant voltage level (V_0). This is the reason why the cumulative consumed current dif-

ference of the former is greater than that of the later. Therefore, by setting the detection starting voltage level of the differential current detection means (circuit) to the set voltage level (V_0) simply to set the predetermined voltage drop relatively differing from the set level (V_0) or the raised voltage level, the current difference between both signal lines, that is, the voltage difference can be detected stably with accuracy, thus minimizing the influence of disturbances such as noise on the result of detection.

The differential current detection means of the semiconductor integrated circuit in this aspect of the present invention has a means for setting the detection starting level, whereby it is possible to set the detection starting voltage level at such a level as is greatly different (parting from the predetermined voltage level) from a preset voltage level (e.g., precharge voltage level) common to both the signal current detection line and the reference current line. The voltage difference between both signal lines at the time the difference therebetween is detected can be made relatively large. Consequently, the detection of the differential current between the current flowing through the signal current detection line and the reference current is most important and a relatively large voltage difference can be secured even when the differential current is reversed where the differential current is minimized. Therefore, the detection of the differential current by the differential current detection means and its reverse timing can be carried out stably and quickly with accuracy.

Fig. 15 shows a specific circuit diagram of a timing control circuit 90 to which the semiconductor integrated circuit in the sixth aspect of the present invention is applied. The timing control circuit 90 of Fig. 15 is applied to the encoder 11 in the second aspect of the present invention shown in Fig. 8 and as it is exactly the same in structure as the timing control circuit 60 of Fig. 10 except for the installation of a transistor 86 as a means for setting the detection starting level, a precharge transistors 78 for respectively precharging the contacts a and b on one respective sides of both signal lines 62, 64, and a transistor 79 for giving both signal lines 62, 64 an equal potential on the other sides thereof. As this timing circuit 90 is capable likewise of detecting the fact that the number of hit signals applied to the gate electrode of the signal voltage application transistor 67b and held by the data latch circuit of the flag register 18 has reached the predetermined value, for example, ultimately one, like component elements are designated by like reference characters and the detailed description thereof will be omitted.

The differential current detection circuit 70 which best features the timing circuit 90 of Fig. 15 comprises a P-channel MOS transistor (PMOS) 86 connected to the power supply at the same potential as the potential at the other ends of both signal lines 62 and 64, for example, 5V, PMOS transistors 80a, 80b connected to this PMOS transistor 86, N-channel MOS transistors (NMOS) 82a, 82b connected to the above-noted transistors in series, and two precharge transistors 83 as PMOSs. The PMOS transistor 86 connected to the power supply forms the means of setting the detection starting level according to the present invention, with its source electrode connected to the power supply and with its gate electrode connected to its own drain electrode. The gate electrodes of the transistors 82a and 80a connected to the first signal line are connected to each other and also to the contact B between the transistors 80b and 82b. Moreover, the gate electrodes of the transistors 82b and 80b connected to the second signal line are connected to each other and also to the contact A between the transistors 80a and 82a. An output line extends from the contact B and is connected via the inverter 84 to the AND circuit 88. The reset signal of the aforementioned flag register 18 is applied to the other input of the AND circuit 88. The output of the AND circuit 88 is connected to the aforementioned flag register 18.

Assuming in this case that the supply voltage V_{dd} to which the source electrode of the PMOS transistor 86 is connected remains at a predetermined potential, for example, 5V and that the threshold value V_{TH} at a predetermined voltage, for example, about 0.7V, the PMOS transistor 86 is held ON on condition that the gate voltage of the PMOS transistor 86 is lower than what results from subtracting the threshold voltage from the supply voltage (V_{dd} - V_{TH}, e.g., 5 - 0.7 = 4.3V) but it will be turned off if the gate voltage thereof exceeds the difference. Therefore, the voltage of the drain electrode connected to the gate electrode rises up to only the supply voltage - threshold voltage (V_{dd} - V_{TH}, e.g., 4.3V). In other words, the PMOS transistor 86 makes the precharge voltage at the contacts A and B the aforementioned V_{dd} - V_{TH} when the voltage is precharged via the precharge transistor 83 and also functions as what reduces the precharge voltage from the supply voltage V_{dd}. As the precharge potential at the contacts A, B lowers, as described in detail later, the precharged gate electrode voltage of the transistors lowers, thus also lowering the potentials of the contacts a and b when either transistor 82a or 82b is turned on at the time of timing detecting operation, that is, lowering the detection starting voltage level. In other words, the PMOS transistor 86 functions as the mean of setting the detection starting level.

Subsequently, the detecting operation of the timing control circuit 90 in this aspect of the present invention will be described as a representative example in a case where the last one of the hit signal of the flag data in the flag register 18, that is, its last hit signal is detected. In this case, the power supply for precharging purposes is at the same potential, for exam-

ple, 5V and flag data having a plurality of hit signals ("1") is held in the flag register 18 on the assumption that the reference current i_r is 1.5 times as great as the drive current i_0 of one current drive circuit 66, that is, set at 1.5 i_0.

With the precharge control signal line 72 at L (low: "0"), both precharge transistor 78 and the transistor 79 at the respective ends of both signal lines 62, 64 are first turned on to precharge the first and second signal lines 62 and 64, consequently contacts a and b at the same potential, for example, the power supply potential (e.g., 5V). Further, both precharge transistors 83 are turned on to precharge the contacts A and B within the differential current detection circuit 70 at H (high) potential (e.g., 4.3V) likewise. Incidentally, the transistors 82a, 82b of the differential current detection circuit 70, the transistors 67a of the whole current drive circuit 66 and the transistor 68a of the reference current drive circuit 68 are held off. While the transistor 86 connected to the power supply initially is held OFF, the threshold voltage keeps its drain potential at supply voltage - threshold voltage (V_{dd} - V_{TH}, e.g., 4.3V). When the drain potential V_{dd} - V_{TH} of the transistor 86 drops as the result of the energized precharge transistor 83, the transistor 86 is turned on to precharge the contacts A, B. The transistor 86 is held ON to keep precharging the contacts A, B until the potential of the contacts A, B, that is, the gate potential of the transistor 86 reaches the precharge voltage, that is, V_{dd} - V_{TH} (e.g., 4.3V) and the transistor 86 is turned off after the precharge voltage has been reached.

With the precharge control signal line 72 at H (high: "1"), the PMOS transistors 78, 79, 83 are subsequently turned off, whereas the NMOS transistors 67d, 69d, 75d, 77d are turned on. Both the two transistors 69a, 69b of the reference current drive circuit 68 are turned on accordingly and the reference current i_r (= 1.5 i_0) flows through the second signal line 64 to lower the potential of the contact b. On the other hand, the transistor 67b having the gate electrode connected to the data latch circuit 18j of the flag register 18 whose flag data has the hit signal "1" out of m+1 of current drive circuits 66 (66_0, 66_0,..., 66_m) is turned on and the transistor 67a is held on, whereby the drive current i_0 flows from the first signal line 62 through the current drive circuit 66j. Since the flag data in the flag register 18 has a plurality of hit signals "1", for example, k ($k \geqq 2$) of hit signals in this case, current of ki_0 flows through the first signal line 62 and the potential of the contact a drops accordingly.

When k is greater than 2, the potential of the contact a drops faster than that of the contact b because current ki_0 flowing through the first signal line 62 is greater than the reference current i_r (= 1.5 i_0) flowing through the second signal line 64. When the difference (gate - source voltage) between the gate potential (potential at the contact B) of NMOS 82a and the source potential (potential of the contact a) becomes greater than the substrate-biased threshold voltage (e.g., 1.4V) of NMOS 82a, that is, when the potential of the contact a drops beyond detection starting voltage V_{ON} (voltage resulting from subtracting the above-noted threshold voltage from the precharge voltage) (for example, if the potential of the contact a drops up to 2.9V when the potential of the contact B is 4.3V), NMOS 82a is turned on and the potential of the contact A drops. However, the potential of the contact b has not yet so much lowered as to turn on NMOS 82b, which remains in the off state accordingly. Although the current flows through both signal lines 62 and 64 then to cause the potential at the contacts A and a to drop further, NMOS 82b keeps the off state as the potential drop at the contact a, that is, at the contact A is greater than the potential drop at the contact b. The contact B thus keeps "1" and "0" is applied by the inverter 84 connected thereto to the AND circuit 88. On the other hand, the contact A remains at "0".

As the plurality of hit signals "1" within the flag register 18 are encoded, they are reset to "0" one after another. When the number of remaining hit signals comes up to one, the timing control circuit 60 according to the present invention performs the detecting operation, that is, first precharges the precharge control signal line 72 by applying "0" and then applying "1" thereto, thus causing the current i_0 and the reference current i_r (= 1.5 i_0) to flow through the first and second signal lines 62, 64 likewise, respectively. Since the current flowing through the second signal line 64 is greater at this time, the potential of the contact b drops faster than that of the contact a and NMOS 82a conversely keeps the off state, whereas NMOS 82b is held ON. Consequently, the potential of the contact B drops to the low level and inverted by the inverter 84 so that "1" is applied to the AND circuit 88. The potential of the contact A is maintained at H (high) potential.

As a result, it is apparent that more than one hit signal "1" is held in the flag register 18 if the output signal from the inverter 84 of the timing control circuit 90 in this aspect of the present invention is "0" and the number of hit signals is one or less if the output signal is "1". When the output signal is changed from "0" to "1", the result of detection, that is, a switch control signal is obtainable from the "1" signal and the reset signal of the flag register 18 by means of the AND circuit 88. Further, this switch control signal may be used to switch the flag data in the flag register 18 over to the flag data in the prefetch circuit 16. Needless to say, the output signal may be fetched from only the contact A or both contacts A and B.

When the timing detecting operation is started in the timing control circuits 90 in this aspect of the present invention, the current corresponding to the number of hit signals ("1") in the flag register 18 flows into

the signal current detection line (the first signal line) 62 and the predetermined reference current into the reference current drive line (the second signal line) 64. Therefore, the differential current detection circuit 70 detects the small potential difference between the contacts a, b resulting from the difference between the currents flowing through both signal lines 62 and 64 as a great potential difference at the contacts A, B one side of which (high potential sides of the contacts a, b) is held at the precharge voltage (e.g., V_{dd}), the other side (low potential sides thereof) being lowered up to the ground level (e.g., 0V).

The subsequent changes of the contacts A and B precharged at the same precharge potential (e.g., 4.3V) are determined by which one of the transistors 82a and 82b is turned on. In other words, the current flows through the first and second signal lines 62 and 64 during the operation of timing detection, thus causing the potentials of the contacts a and b of both signal lines 62, 64 to drop as previously noted. When either one of the potential difference between the contacts B and a and the potential difference between the contacts A and b exceeds the substrate-biased threshold value (e.g., 1.4V), that is, when either one of the potentials of both signal lines 62 and 64 (those of the contacts a and b) drops beyond the detection starting voltage (potential resulting from subtracting the aforementioned threshold voltage from the precharge potential) V_{ON} (e.g., 2.9V), one of the transistors 82a and 82b is turned on. As a result, the contact A or B on the side of the energized transistor 82a or 82b immediately becomes equal in potential to the contact a or b thus lowered and lowers up to the ground level (0V) together. On the other hand, the contact A or B on the side of the de-energized transistor 82a or 82b is maintained at the precharge potential (4.3V).

It is thus possible to detect the predetermined number of hit signals (e.g., ultimately only one) by making the potential of the contact B a detection signal and by taking out the output signal via the inverter 84. In other words, the transistor 82b is turned on as the inverter 84 has been connected to the tip of the contact B and the potential of the contact B then drops. When the potential becomes lower than the threshold value (e.g., about 2.5V) of the inverter 84, the output signal "1" is obtained.

If the potential difference between the contacts a and b is excessively small when the contacts A and B branch off in the differential current detection circuit 70, the ON-operation of the transistors 82a and 82b becomes irrelevant to the potential difference between the contacts a, b, that is, the possibility of malfunction increases. Therefore, the greater the potential difference between both contacts a and b, the less the transistors may be seriously affected thereby. Stable accurate timing detection is thus always assured.

The equally precharged potential at the contacts a, b of both signal lines 62, 64 lowers likewise as the temporary inflow of charge into the control transistors 67a, 69a, 75a, 77a that have turned on the current drive circuit 66, the reference current drive circuit 68, the dummy circuits 74, 76 and the like in the initial stage of the timing detecting operation (at the time the precharge control signal line 72 is at the high level (H: "1")). However, the difference between the whole signal current i flowing in the first signal line 62 through the current drive circuit 66 turned on by the signal voltage application transistor 67b in proportion to the number of hit signals ("1") held in the flag register 18 and the reference current i_r flowing in the second signal line 64 through the reference current drive circuit 68 turned on by the transistor 69b causes potential difference at the contacts a and b because of the current difference after the passage of fixed time followed by the commencement of detection. The greater the difference between the cumulative currents that have flowed down both signal lines 62, 64, the greater the potential difference becomes, so that the potential difference grows until the predetermined time after the commencement of detection. As the current flows, the potential of both signal lines 62, 64 thus precharged lowers and the charge held thereby decreases and when the potential comes almost near to the ground level, the current becomes hard to flow and ultimately stops flowing. Consequently, the potentials of both signal lines, that is, the potentials at both contacts a, b are set at substantially the same ground level after the passage of adequate time.

Unless the potential of the contacts a and b has lowered up to the ground level according to the present invention, the lower their potential than the precharged one, the greater the difference in potential between the contacts a and b becomes. Consequently, it is preferred to make the lower one of the potentials of the contacts a and b a detection starting voltage for use in turning on either transistor 82a or 82b, that is, to make greater the difference between the precharge voltage of both contacts a and b, or both signal lines 62 and 64, and the level of the detection starting voltage for turning on the transistors 82a, 82b, at a point of time a greater potential difference occurs between both contacts a and b. For this reason, there is a method of either increasing the precharge voltage of both signal lines 62, 64 or lowering the detection starting voltage level. In order to raise the precharge voltage of both signal lines 62, 64, a step-up circuit may be employed. However, an increase in not only the circuit area but also cost resulting from the provision of such a step-up circuit makes it desirable to provide a means to lower the detection starting voltage level. Since the detection starting voltage is the source voltage at which the transistor 82a or 82b is turned on, that is, what is at the potential of the contacts a or b and since the threshold voltage

(e.g., 1.4V) between the gate-source of the transistors 82a, 82b has been predetermined, the detection starting voltage level may be lowered by lowering the potential of the gate electrodes of the transistors 82a, 82b.

In the timing control circuit 90 of Fig. 15, the precharge potential of the contacts A, B connected to the gate electrodes of both transistors 82a, 82b is reduced by the threshold voltage of the PMOS transistor from the supply potential (e.g., 5V) up to a predetermined potential (e.g., 4.3V) by means of a transistor 86 for setting the detection starting level using the PMOS transistor. However, the present invention is not limited to the arrangement above but can employ the detection starting level setting transistor 86 formed with an NMOS transistor as in the case of a timing control circuit 92 of Fig. 16. Assuming the substrate-biased gate - source threshold voltage V_{TM} of the NMOS transistor is about 1.4V, for example, a rise in the potential of the source electrode may be reduced up to V_{dd} - V_{TH}, that is, about 3.6V by connecting the drain electrode of the NMOS transistor 86 to its gate electrode when the current voltage V_{dd} is 5V. Consequently, the precharge voltage of the contacts A, B is maintained at about 3.6V and since the threshold voltage V_{TH} between the gate - source of the NMOS transistors 82a, 82b is about 1.4V, the detection starting voltage V_{ON} at which these transistors 82a, 82b are turned on may be set at about 2.2V (3.6 - 1.4V).

When the semiconductor integrated circuit according to the present invention is applied as a timing control circuit of the encoder in order to increase the difference between the contacts a and b of both signal lines 62, 64 quickly even though a decrease in the potential between the contacts a and b is insignificant after the timing detecting operation is started, there may be installed the signal voltage application transistor 67c of the current drive circuit 66 on the side of the first signal line (signal current detection line) 62, the control transistor 67d on the grounding side as in a timing control circuit 92, unlike the timing control circuit 90 of Fig. 15, the gate-grounded transistor 75c of the dummy circuit 74 on the second signal line (reference current drive line) side, and the control transistor 75d on the grounding side. Only the control transistor 67d of the current drive circuit 66 is turned on when the signal voltage application transistor 67c is turned on, whereas the whole control transistor 67d at the time the transistor 67c is not turned on and the control transistor 75d of the whole dummy circuit 74 are not turned on, whereby it is possible to eliminate the charge flowing into these control transistors 67d, 75d in the initial stage of the timing detecting operation, to prevent the potentials of both signal lines 62, 64, that is, both contacts a and b from simultaneously dropping in the initial stage of the timing detecting operation, and to increase the potential difference itself between both contacts a and b.

In the case of the timing control circuit 60 of Fig. 10, however, the contacts A, B are precharged at the supply potential V_{dd} (e.g., 5V) since the precharge transistor 83 is connected to the power supply. As the precharge voltage of the contacts A, B is at the supply potential V_{dd}, the detection starting voltage V_{ON} at which the transistors 82a, 82b whose gate - source threshold voltage is V_{TH} (e.g., 1.4V) are turned on conforms to V_{dd} - V_{TH} (e.g., 3.6V). On the contrary, as the detection starting levels (voltage) V_{ON} of the timing control circuits 90 and 92 shown in Figs. 15 and 16 in the present aspect of the invention respectively remain to be about 2.9V and 2.2V against the same supply potential (5v), it is possible to lower the detection starting voltage level V_{ON} as compared with the timing control circuit 60 of Fig. 10. Consequently, the potential difference between both signal lines 62 and 64, that is, contacts a and b is increased further, whereby the transistor 82a or 82b can be turned on stably with accuracy at a lower potential. As a result, the timing control circuits 90 and 92 of Figs. 15 and 16 in this aspect of the present invention have a greater noise margin and consequently the differential current detection circuit 70, even if subjected to noise influence, may less malfunction to ensure accurate stable timing detection at all times.

Figs. 17(a), (b) show simulation waveforms relating to the operation of the timing control circuit 92 shown in Fig. 16 and that of the timing control circuit 60 shown in Fig. 10, respectively.

The voltage difference between the nodes a and b at the operating points where the nodes A and B branch off is 0.6V in the case of Fig. 17(a) and 0.1V in Fig. 17(b), indicating a greater margin in the former.

The timing control circuit applied to the encoder in the second aspect of the present invention is basically thus arranged.

Since the main encoder 12 of the encoder 11 of Fig. 8 to which the timing control circuit 90 in this aspect of the present invention is applied operates likewise as shown in the timing chart of Fig. 13, the description thereof will be omitted.

As set forth above in detail, the detection start level setting means for making relatively greater the difference between the detection start voltage and what is preset to the first and second signal lines is provided for the differential current detection means in the semiconductor integrated circuit in the sixth aspect of the present invention. Therefore, the potentials of both signal lines, that is, the signal current detection line and the reference current drive line are sufficiently lowered at the timing of detecting operation and the potential difference can be detected dynamically when the difference grows sufficiently greater. Consequently, it is possible to detect the differential current between the reference current drive line and the signal current detection line stably and

quickly with accuracy by a greater noise margin at low power consumption. In addition, the circuitry can be made compact in configuration to ensure that the semiconductor integrated circuit in this aspect of the present invention is fit for use as a timing control circuit for previously notifying the termination of the encoding operation in an encoder for CAM.

Referring to Figs. 18 - 22, a semiconductor integrated circuit in the seventh, eighth and ninth aspects of the present invention will be described in detail. The semiconductor integrated circuits in these aspects of the present invention are applicable to the encoder in the second aspect thereof as number detection circuits for timing control.

In the semiconductor integrated circuits in the seventh, eighth and ninth aspects of the present invention, there is preset the reference current ir made to flow in the reference current drive means provided on the reference current drive line as the second signal line in accordance with the number of data k_0 ($M > k_0 \geqq 0$) desired to be detected out of the data "1" or "0" fed to data input lines for respectively controlling M ($M \geqq 1$) provided in parallel on the first signal line, or the signal current detection line, that is, a current value ($k_0 i_0 < i_r < (k_0 + 1) i_0$) greater by k_0 times and smaller by $k_0 + 1$ times than the current value i_0 flowing through one current drive means. Prior to the detecting operation, moreover, the first and second signal lines are precharged at the predetermined same potential. Therefore, the inputs and inverted outputs of the first and second invertors both connected to these signal lines in series or parallel are identical and both inputs to the differential current detection means are also identical.

Therefore, the operating timing is set in the semiconductor integrated circuit in this aspect of the present invention and when the whole current drive means with the data input line supplied with the desired data becomes active, reference current i_r flows through the current drive means and current i_0 flows through each current drive means. Further, current i ($i = ki_0$) in proportion to the number k ($M > k \geqq 0$) flows through the signal current detection line. On the other hand, reference current i_r is caused by the reference current drive means to flow through the reference current drive line. As a result, the potentials of the signal current detection line and the reference current drive line that have been precharged at the predetermined potential start decreasing. When k is greater than k_0 in the current drive means kept active, the potential of the signal current detection line lowers faster and when it is less than k_0, that of the reference current drive line lowers faster.

When the potential of either signal line lowers beyond the threshold value of the inverter connected thereto in the semiconductor integrated circuit according to the present invention, the output of the inverter is inverted. In the semiconductor integrated circuit in the seventh aspect of the present invention, the differential current detection means is capable of directly detecting the inversion of the inverted output of the inverter connected to the signal line in series. In the eighth and ninth aspects of the present invention, moreover, the inversion of the inverted output of the inverter connected to the signal line in parallel caused the transistor connected to the signal line (connected to the inverter in parallel) to be turned on, letting the current flow through the signal line to lower the potential and making the differential current detection means detect the reduction of the input potential. Consequently, the differential current between the current values i and i_r flowing through the first and second signal lines is detected by the differential current detection means, so that the inversion of a differential current code, that is, the inversion (timing) of the size relation between both current values i and i_r is output. In this way, it is detected that the number k of desired data out of those applied to each data input line has reached the preset number k_0 of data to be detected. The semiconductor integrated circuit according to the present invention can thus detect the number of desired data fed to the data input line.

By regulating the threshold values of the invertors connected to the respective signal lines, a relatively great potential difference between both signal lines can be secured when the differential current therebetween is detected. Accordingly, the inverted output of only one inverter can be inverted then quickly with accuracy. Since the inverter itself has drive capability in the seventh aspect of the present invention, moreover, the voltage level of the initial value of the input signal to the differential current detection means can be raised by the inversion of the inverter on one side and the voltage difference between two input signals due to the differential current between both signal lines can be made greater at the start of detection to ensure that the detecting operation is performed with stability. Since the transistor is turned on by inverting the inverter to ensure that one of the signal lines is conducted to the input of the differential current detection means in the eighth and nineth aspects of the present invention, the detecting operation is performed stably with accuracy. Consequently, it is possible to detect by the differential current detection means the inversion of the differential current between both signal lines stably and quickly with accuracy.

Fig. 18 shows a specific circuit diagram of a timing control circuit 100 to which the semiconductor integrated circuit in the seventh aspect of the present invention is applied. The timing control circuit 100 of Fig. 18 is applied to the encoder 11 in the second aspect of the present invention shown in Fig. 8 and as it is exactly the same in structure as the timing control circuit 61 of Fig. 12 in the fifth aspect of the present invention except for the installation of a transistor 86

as a means for setting the detection starting level, a precharge transistors 78 for a train of invertors 102a, 104a and 102b, 104b, and transistors 103a, 103b, like component elements are designated by like reference characters and the detailed description thereof will be omitted.

The timing control circuit 100 of Fig. 18 in this aspect of the present invention comprises a first signal line (signal current detection line) 62, a second signal line (reference current drive line) 64, m+1 of current drive circuits (current drive means) 66_0, 66_1,..., 66_m provided for respective m+1 of data latch circuits 180, 18_1,..., 18_m of a flag register 18 in parallel to the first signal line 62, a reference current drive circuit (reference current drive means) provided for the second signal line 64, a differential current detection circuit (differential current detection means) 70 for detecting the difference between the currents flowing through the first and second signal lines 62, 64, that is, detecting the differential current, invertors 102a, 104a and 102b, 104b provided between the first and second signal lines 62, 64 and the differential current detection circuit 70, and a precharge control signal line 72 for controlling the operation timing of the timing control circuit, namely, the current drive circuits 66 (66_0, 66_1,..., 66_m), the reference current drive circuit 68 and the differential current detection circuit 70.

In the timing control circuit 100, contacts p and q at one ends of the respective first and second signal lines 62 and 64 are connected to the respective invertors 102a and 102b and further connected via the invertors 104a and 104b to the differential current detection circuit 70 at the contacts a and b, the other ends thereof being connected via respective precharge transistors 78 to a power supply at a predetermined potential, for example, 5V. In this case, the value i_r of the reference current caused to flow down the reference current drive circuit 68 may properly be determined according to the value i_0 of the current that can be made to flow by the current drive circuit 66 (66_0, 66_1,..., 66_m) and the number of hit signals to be detected, and may be greater than i_0 but less than $2i_0$ and the value at which the inversion timing of the invertors 102a and 102b is clearly distinguishable and at which the differential current detection circuit 70 is able to detect the differential current in order for the last one of the hit signal to be detected.

The invertors 102a and 104a are connected between the first signal 62 and the differential current detection circuit 70, whereas the invertors 102b and 104b are connected between the second signal line 64 and the differential current detection circuit 70. Moreover, NMOS transistors 103a and 103b connected to a predetermine potential (e.g., grounding potential) are connected in between the invertors 102a, 104a and 102b, 104b, respectively. These gate electrodes are also connected to the contact a (between the inverter 104a and the differential current detection circuit 70) and the contact b (between the inverter 104b and the differential current detection circuit 70). The threshold voltage at which the outputs of the invertors 102a and 102b are inverted is regulated in accordance with the width or threshold voltage of PMOS and NMOS transistors constituting the inverter. By regulating the threshold voltage for the output inversion, it is possible to secure a relatively great potential difference due to the differential current between the contacts p and q and to increase the operating margin.

Subsequently, the detecting operation of the timing control circuit 100 according the present invention will be described as a representative example in a case where the last one of the hit signal of the flag data in the flag register 18, that is, its last hit signal is detected. In this case, flag data having a plurality of hit signals ("1") is held in the flag register 18 on the assumption that the reference current ir is 1.5 times as great as the drive current i_0 of one current drive circuit 66, that is, set at 1.5 i_0.

With the precharge control signal line 72 set at L (low: "0"), prior to start the detecting operation, both precharge transistor 78 and the transistor 79 are first turned on to precharge the first and second signal lines 62 and 64, consequently contacts p and q at the same H (high) potential (e.g., 5V). Further, both precharge transistors 83 are turned on to precharge the contacts A and B within the differential current detection circuit 70 at H (high) potential (e.g., 5V) likewise. Consequently, the invertors 102a and 102b set both connections between the invertors 102a, 104a and 102b, 104b at L (low) potential, whereas the invertors 104a and 104b set the contacts a and b at H (high) potential. The transistors 103a and 103b are thus turned on to ensure that both connection potentials between the invertors 102a, 104a and 102b, 104b are set at L (low) potential. Incidentally, the transistors 82a, 82b of the differential current detection circuit 70, the transistors 67d of the whole current drive circuit 66 and the transistor 69d of the reference current drive circuit 68 are held off.

With the precharge control signal line 72 at H (high: "1"), the PMOS transistors 78, 83 are subsequently turned off, whereas the NMOS transistors 67d, 69d, 75d, 77d are turned on. Both the two transistors 69c, 69d of the reference current drive circuit 68 are turned on accordingly and the reference current i_r (= 1.5 i_0) flows through the second signal line 64 to lower the potential of the contact q. On the other hand, the transistor 67c having the gate electrode connected to the data latch circuit 18j of the flag register 18 whose flag data has the hit signal "1" out of m+1 of current drive circuits 66 (66_0, 66_0,..., 66_m) is turned on and the transistor 67d is held on, whereby the drive current i_0 flows from the first signal line 62 through the current drive circuit 66j. Since the flag data in the flag register 18 has a plurality of hit signals

"1", for example, k ($k \geqq 2$) of hit signals in this case, current of ki_0 flows through the first signal line 62 and the potential of the contact p drops accordingly.

When k is greater than 2, the potential of the contact p drops faster than that of the contact q because current ki_0 flowing through the first signal line 62 is greater than the reference current i_r (= 1.5 i_0) flowing through the second signal line 64. Therefore, the output inverted potential (threshold value) is reached at the contact p earlier than the contact q and the output inversion of the inverter 102a occurs earlier than that of the inverter 102b and besides the output inversion of the inverter 104a occurs earlier. In other words, only the invertors 102a and 104a undergo the output inversion earlier, thus causing the potential of the contact a to drop. When the difference between the gate potential (potential at the contact B) of NMOS 82a and the source potential (potential of the contact a) in the differential current detection circuit 70 becomes greater than the substrate-biased threshold voltage (e.g., 1.4V) of NMOS 82a (for example, the potential of the contact a drops up to 3.6V when the potential of the contact B is 5V), NMOS 82a is turned on and the potential of the contact A drops and turns out to be in the L (low) state. As the potential of the contact a drops, NMOS 103a is turned off to keep the connection with the invertors 102a and 102b in the H (high) state. On the other hand, the contact q (the second signal line 64) has not yet reached the output inverted potential (threshold value) of the inverter 102b and the output inversion of both invertors 102b and 104b does not occur. The potential of the contact b is thus maintained in the H (high) state and NMOS 82b remains in the OFF state, whereas the contact B is maintained in the H (high) state.

The current then flows through both signal lines 62 and 64, causing the potentials of the contacts p and q to lower. The potential of the contact q drops beyond the threshold value of the inverter 102b, causing the output inversion thereof and the output inversion of the inverter 104b. Since the gate potential (potential of the contact A) NMOS 82b is maintained in the L (low) state even though the potential of the contact b drops, NMOS 82b is maintained in the OFF state and the potential of the contact B is maintained in the H (high) state. The latch operation of the differential current detection circuit 70 keeps the setting at H (high) "1", which is inverted by the inverter 84 connected thereto, and L (low) "0" is applied to the AND circuit 88. On the other hand, the contact A remains at L (low) "0".

As the plurality of hit signals "1" within the flag register 18 are encoded, they are reset to "0" one after another. When the number of remaining hit signals comes up to one, the timing control circuit 100 according to the present invention performs the detecting operation, that is, first precharges the precharge control signal line 72 by applying "0" and then applying "1" thereto, thus causing the current i_0 and the reference current i_r (= 1.5 i_0) to flow through the first and second signal lines 62, 64 likewise, respectively. Since the current flowing through the second signal line 64 is greater at this time, the potential of the contact q drops faster than that of the contact p and the output inversion of the invertors 102b and 104b conversely occurs earlier. Only the potential of the contact b drops first and NMOS 82b is turned on, whereas NMOS 82a remains in the OFF state. Consequently, the potential of the contact B drops to L (low) level and inverted by the inverter 84 so that "1" is applied to the AND circuit 88. The potential of the contact A is maintained at H (high) potential.

As a result, it is apparent that more than one hit signal "1" is held in the flag register 18 if the output signal from the inverter 84 of the timing control circuit 100 in this aspect of the present invention is "0" and the number of hit signals is one or less if the output signal is "1". When the output signal is changed from "0" to "1", the result of detection, that is, a switch control signal is obtainable from the "1" signal and the reset signal of the flag register 18 by means of the AND circuit 88. Further, this switch control signal may be used to switch the flag data in the flag register 18 over to the flag data in the prefetch circuit 16. Needless to say, the output signal may be fetched from only the contact A or both contacts A and B.

By regulating the threshold values of the invertors 102a and 104b connected to both signal lines 62 and 64, the difference in potential drop between both contacts p and q resulting from the differential current between both signal lines 62 and 64, even though it is small, can be detected to ensure that the output of the inverter on only one side is inverted first at all times. Since the inverter itself has drive capability, the potential of the contacts a and b can be raised by the output inversion and the great potential difference between the contacts a and b can be secured when the detecting operation is started by the differential current detection circuit 70 to ensure that either NMOS 82a or 82b is turned on. Therefore, the detecting operation of the differential current detection circuit 70 can be performed stably and certainly. Since the potential difference between the contacts a and b is greater than the potential difference between the contacts p and q at the time the detecting operation is started by the differential current detection circuit 70, either of the transistors 82a and 82b is prevented from malfunctioning. As the timing circuit to which the semiconductor integrated circuit in the seventh aspect of the present invention is applied has a greater noise margin and is hardly affected by noise, it can make timing detection stably with accuracy at all times. By regulating the input threshold voltage for varying the outputs of the invertors 102a, 102b in such a way as to keep the voltage lower, it is needless to say possible to ensure stable operations by in-

creasing the voltage difference between the contacts p and q when one of the invertors starts to operate.

The timing circuit 100 as illustrated is arranged so as to use two-stage invertors 102a, 104a and 102b, 104b provided between both signal lines 62 and 64 and the differential current detection circuit 70 and to perform the detecting operations by making NMOS 82a and 82b drop the potential of either contact A or B. However, the present invention is not limited to this arrangement but may be practiced by providing one-stage invertors and a differential current detection circuit for raising the potential of either contact A or B by means of PMOS transistors.

The timing control circuit 100 with the semiconductor integrated circuit applied thereto is basically so configured as stated above in the seventh aspect of the present invention.

A description will subsequently be given of a semiconductor integrated circuit in the eighth aspect of the present invention.

Fig. 19 shows a timing control circuit to which the semiconductor integrated circuit in the eighth aspect of the present invention is applied. As the timing control circuit 106 of Fig. 19 is exactly the same in structure as the timing control circuit 100 of Fig. 18 except for the installation of invertors 108a, 108b and transistors 109a, 109b in place of the two-stage invertors 102a, 104a and 102b, 104b, like component elements are designated by like reference characters and the detailed description thereof will be omitted.

In the timing control circuit 106 of Fig. 19, the NMOS transistor 109a is connected between the contact p at one end of the first signal line 62 and the contact a on the source electrode side of NMOS 82a of the differential current detection circuit 70; the inverter 108a between the gate electrode of NMOS 109a and the contact p; the NMOS transistor 109b between the contact q at the end of the second signal line and the contact b on the source electrode side of NMOS 82b; and the inverter 108b between the gate electrode of NMOS 109b and the contact q. In this case, the threshold values of the invertors 108a and 108b are regulated like the invertors 102a and 102b.

Like the timing control circuit 100 of Fig. 18, the timing control circuit 106 is such that all the contacts A, B, a, b, p, q are first precharged by the L signal of the precharge control signal line 72 at H level (for example, the contacts A, B, p, q at the supply voltage (Vdd, e.g., 5V) and the contacts a and b at 3.6V by the substrate-biased threshold value (e.g., 1.4V) of NMOS 82a, 82b). With the signal line 72 as H, ki_0 current lead-in corresponding to the number k of hit signals is subsequently caused to occur on the first signal line 62 by the current drive circuit 66 which is made active by the hit signal "1" of the flag register 18 and the voltage drops correspondingly. Then i_r ($1.5i_0$) current lead-in is caused to occur on the second signal line 64 by the reference current drive line 68.

When the number k of active current drive circuits 66 is more than one, the voltage of the first signal line 62 then drops faster than that of the second signal line 64. Consequently, the threshold voltage of the inverter is reached at the contact b earlier than at the contact q and the output inversion of the inverter 108a occurs earlier than that of the inverter 108b. Therefore, NMOS 109a is turned on before NMOS 109b. Then a voltage drop occurs at the contact a and NMOS 82a of the differential current detection circuit 70 is turned on and further the potential of the contact A is set at L (low) level. As a result, the potential of the contact q then lowers further and the output of inverter 108b is inverted and the transistor 109b is turned on. Even though the potential of the contact b drops, NMOS 82b remains in the off state and the potential of the contact B remains in the H state as the gate potential (potential of the contact A) of NMOS 82b is already at L. Consequently, the output at the contact B is inverted by the inverter 84 and the output of the inverter 84 as the output of the timing control circuit 106 is held L (low).

When the number k of active current drive circuits 66 is conversely one or less, the flow down current i of the first signal line 62 is greater than the flow down current i_r of the second signal line 64 and the voltage drop at the contact p is greater than the voltage drop at the contact q. Therefore, the output of the inverter 108b is inverted and the transistor 109b is turned on and further the voltage drop at the contact b occurs. Subsequently, NMOS 82b is turned on and the potential of the contact B is set at L level. Since the potential of the gate electrode (contact B) of NMOS 82a is at L level, on the other hand, NMOS 82a is never turned on, irrespective of the potential of the contact a, that is, despite the fact that the potential drop occurs at the contact q, that the output of the inverter 108a is inverted and that the potential of the contact a drops when the transistor 109a is turned on. The potential of the contact A is maintained at H level. As a result, the potential of the contact B is inverted by the inverter 84 and the output of the timing control circuit 106 is changed to H level. It is thus detected that the number of hit signals "1" in the flag register 18 ultimately comes up to one.

By regulating the threshold values of the invertors 108a and 108b in the timing control circuit 106 as illustrated, the potential difference between the contacts a and b can be set when the detecting operation is started by the differential current detection circuit 70, that is, at a point of them either NMOS 82a or 82b is turned on. Consequently, timing detection can be made with a greater noise margin stably and accurately at all times.

Fig. 20 shows a timing control circuit to which the semiconductor integrated circuit in the ninth aspect of the present invention is applied. The timing control

circuit 110 of Fig. 20 is additionally provided with precharge PMOS transistors 78, 78 for precharging contacts a and b at up to a predetermined potential, for example, supply potential V_{dd} (e.g., 5V) and PMOS 79 for connecting both contacts a and b to make these contacts equipotential in the timing control circuit 106. The gate electrodes of these PMOS 78, 78, 79 are connected to a precharge control line 72.

When the contacts A, B, p, q are first precharged at H level, for example, the supply potential 5V, the potentials of the contacts a and b are also set at H level of 3.6V in the timing control circuit 106 of Fig. 19, whereas the potentials of the contacts a and b can be raised up to 5V in the timing control circuit 110 of Fig. 20. Therefore, the potential difference between the contacts p and q can be made greater than what is set in the timing control circuit 106 of Fig. 19 at a point of time the detecting operation is started by the differential current detection circuit 70, that is, at the point of time either MNOS 82a or 82b is turned on. The timing control circuit 110 of Fig. 20 has a further greater noise margin to ensure accurate, stable timing detection at all times.

Moreover, use may needless to say be made of control transistors 67e, 77e merging the control transistors 67d, 69d, 75d, 77d of the current drive circuit 66 and the reference current drive circuit 68 for common use as in the case of timing control circuit 112 of Fig. 21.

An OR logical circuit 114 that has received an initial value setting signal of Fig. 22 is inserted between the AND circuit 88 and the flag register 18 so as to set the initial value of the flag register 18.

As the encoding operation of the main encoder 12 of the encoder 11 of Fig. 8 to which the timing control circuits 100, 106, 110, 112 in this aspect of the present invention is similar to what is illustrated by reference to the timing chart of Fig. 13, the description thereof will be omitted.

The timing control circuits with the applications of the semiconductor integrated circuits are basically so configured as stated above in the eighth and ninth aspects of the present invention.

In the semiconductor integrated circuits in the seventh, eighth and ninth aspects of the present invention, the invertors are provided in series or parallel between the first and second signal lines and the differential current detection means and by regulating the threshold voltage of the inverted output of the inverter, the potential difference between two input signals to the differential current detection means when the detecting operation is started by the differential current detection means can be set relatively optionally, so that the differential current detection means is prevented from detection failure and malfunction. It is therefore possible according to the present invention to detect the size of the differential current between both signal lines and reverse timing stably with accuracy at all times. In other words, the semiconductor integrated circuits according to the present invention are hardly affected by noise and stable circuits having a greater operating margin and consequently fit for use as timing control circuits for previously notifying or predicting the termination of the encoding operation in encoders of content addressable memories.

In the seventh aspect of the present invention, the differential current detection means can be made to perform the detecting operation after the output of the inverter is inverted, regardless of potential changes on the first and second signal lines. In ninth aspect of the present invention, moreover, an operating margin can be made greater than that in the eighth aspect thereof.

Referring to Fig. 23, a semiconductor integrated circuit in the tenth aspects of the present invention will be described in detail. The semiconductor integrated circuit in this aspect of the present invention is applicable to the encoder in the second aspect thereof as a number detection circuit for timing control.

In the semiconductor integrated circuit in this aspect of the present invention, a reference current control register is made to hold the number of data equal to that of data k_0 ($M > k_0 \geqq 0$: wherein M ($M \geqq 1$): the number of data that can be held in a data register) desired to be detected out of the data "1" or "0" held in the data register. For example, the reference current control register is made to hold k_0 of data "1" if it is desired to detect that the number of data "1" held in the data register comes to k_0.

The current flowing through M of signal unit current drive means provided in parallel to the first signal line, that is, the signal current detection line and controlled by the data held in the data register and the current flowing through N of reference unit current drive means provided in parallel to the reference current drive line as the second signal line and controlled by the data held in the reference current control register are defined as an identical unit current i_0 and an offset current i_{0s} flowing through a reference offset current drive means provided in the reference current drive line is preset as what is smaller in current value ($i_0 > i_{0s} > 0$) than the unit current i_0. Therefore, a reference current i_r ($= k_0 i_0 + i_{0s}$) has a value greater than $k_0 i_0$ and smaller than $(k_0 + 1) i_0$, namely, ($k_0 i_0 < i_r < (k_0 + 1) i_0$).

In the semiconductor integrated circuit according to the present invention, the unit current i_0 flows through each of the signal unit current drive means corresponding to the data register holding desired data when the operating timing is set. Consequently, the current i ($i = ki_0$) corresponding to the number k ($M > k \geqq 0$) flows through the signal current detection line, whereas the reference current i_r flows through the reference current drive line. The differential current detection means is then used to detect the dif-

ferential current between the current i and i_r flowing through both signal lines and output an inverted differential current code, that is, inversion (timing) of the size relation between both current values i and i_r. In this manner, it is detected that the number k of desired data output of the data input to each data input line has reached the number k_0. The semiconductor integrated circuit according to the present invention is capable of detecting the number of desired data held in the data register. Moreover, the number of data to be detected may be set optionally by changing the number of desired data set and held in the reference current control register.

Fig. 23 shows a specific circuit diagram of a timing control circuit 116 to which the semiconductor integrated circuit according to the present invention is applied. The timing control circuit 116 of Fig. 23 is applied to the encoder 11 in the second aspect of the present invention shown in Fig. 8 and as it is exactly the same in structure as the timing control circuit 61 of Fig. 12 in the fifth aspect of the present invention except for the installation of a reference current control register 118 and an OR circuit 114, like component elements are designated by like reference characters and the detailed description thereof will be omitted. In the timing control circuit 61 of Fig. 12, the serially-connected transistors 75c and 75d are used as dummy circuits 74, whereas in the timing control circuit 116 of Fig. 23 in this aspect of the present invention, the gate of the NMOS transistor 75c is connected to the output of the reference current control register 118 and the transistor is made to function as a signal unit current drive circuit 74.

The timing control circuit 116 of Fig. 23 according to the present invention comprises a reference current control register 118 having m+1 of data latch circuits 118_0, 118_1,..., 118_m, a first signal line (signal current detection line) 62, a second signal line (reference current drive line) 64, m+1 of signal unit current drive circuits (signal unit current drive means) 66_0, 66_1,..., 66_m provided for respective data latch circuits 18_0, 18_1,..., 18_m of a flag register 18 in parallel to the first signal line 62, m+1 of reference unit current drive circuits (reference unit current drive means) 74_0, 74_1,..., 74_m provided for respective data latch circuits 118_0, 118_1,..., 118_m of the reference current control register 118 in parallel to the second signal line, a reference offset current drive circuit (reference offset current drive means) 68 provided for the second signal line 64, a differential current detection circuit (differential current detection means) 70 for detecting the difference between the currents flowing through the first and second signal lines 62, 64, that is, detecting the differential current, and a precharge control signal line 72 for controlling the operating timing of the timing control circuit, namely, the unit current drive circuits 66 (66_0, 66_1,..., 66_m), 74 (74_0, 74_1,..., 74_m), the reference offset current drive circuit 68 and the differential current detection circuit 70.

The reference current control register 118 is similar in structure to the flag register 18 and has m+1 of data latch circuits 118_0, 118_1,..., 118_m and makes k_0 of data latch circuits 118_i hold k_0 of data (hit signal) "1" in accordance with k_0 ($m+1 > k_0 \geqq 0$) of flag data (hit signal "1") to be detected and held in the respective data latch circuits 18_0, 18_1,..., 18_m of the flag register 18. The number of data (hit signal) "1" to be held in the data latch circuit of the register 118 can be set optionally from the outside, and the number k_0 to be detected can also be set optionally as occasion demands. Moreover, it is optional to decide which k_0 of data latch circuits 118_j out of the those 118_0, 118_1,..., 118_m of the register 118 should hold the data "1".

The reference unit current drive circuit 74 is exactly the same in structure as the unit current drive circuit 66 and comprises the signal application transistor 75c and the control transistor 75d, these being formed with two of serially-connected N-channel MOS transistors one side of which is connected to the second signal line 64, the other being grounded. The gate electrode of the signal application transistor 75c on the side of the signal line 64 is connected to the output terminal Q of the data latch circuit 118_j corresponding to the reference current control register 118, whereas the gate electrode of the control transistor 75d on the grounding side is connected to the control signal line 72. Moreover, the unit current drive circuit 74, like the unit current drive circuit 66, is so arranged as to let the unit current i_0 flow from the second signal line 64 when the control transistor 75d is turned on during the detecting operation and when the signal application transistor 75c is turned on simultaneously with receipt of the hit signal "1" at its gate electrode from the reference current control register 118. When the number of hit signals to be detected is k_0, k_0 of hit signals "1" are held in the reference current control register 118. Consequently, k_0 of reference unit current drive circuits 74 are turned on and k_0 i_0 of currents in the whole circuit flow through the second signal line. The unit currents i_0 are arranged so that they are identical in all the unit current drive circuits 66_0, 66_1,..., 66_m and 74_0, 74_1,..., 74_m. In this case, however, variations of transistors 67c, 67d and 75c, 75d for use may be ignored on condition that the variations thereof are produced during the course of processing.

On the other hand, the reference offset current drive circuit 68 is used for the predetermined reference offset current i_{0s} to flow through the second signal line The value of the reference offset current i_{0s} may be smaller ($i_0 > i_{0s} > 0$) than that of the unit current i_0 and may be a value at which the differential current detection circuit 70 is able to detect the differential current. This current value i_{0s} may be determined in consideration of the unit current i_0 and variations of circuit elements such as the transistors 67c,

67d, 75c, 75d constituting the unit current drive circuits 66 and 74, the transistors 69c, 69d constituting the reference offset current drive circuit 68. It should preferably be $i_{0s} = 0.2\ i_0 - 0.8\ i_0$, for example.

As a result, the value of the reference current i_r flowing through the second signal line at the time of detection is given as the sum ($k_0\ i_0 + i_{0s}$) of the value $k_0\ i_0$ of the current flowing through k_0 of unit current drive circuits 74 which are turned on in accordance with the number (of hit signals to be detected) k_0 and the value i_{0s} of the reference offset current flowing through the reference offset current drive circuit 68. The current value ($k_0\ i_0 < i_r < (k_0 + 1)\ i_0$) is greater than what is k_0 times the unit current value i_0 and smaller than what is $k_0 + 1$ times. For example, the reference current value i_r is greater than i_0 and smaller than $2i_0$ in order to detect the last one of the hit signal but should be set at $i_r = 1.2\ i_0 - 1.8\ i_0$ in consideration of variations of component circuit elements and a margin in the differential current detection circuit 70.

The output of the AND circuit 88 of the differential current detection circuit 70 is connected to the clock terminal of the flag register 18. Moreover, the output of the AND circuit is connected to the one input of an OR circuit 114 and the other input of the OR circuit 114 is connected to an initial value setting signal.

Subsequently, the detecting operation of the timing control circuit 116 according the present invention will be described as a representative example in a case where the last one of the hit signal of the flag data in the flag register 18, that is, its last hit signal is detected. In this case, flag data having hit signals ("1") in the plurality of data latch circuits 18_j is held in the flag register 18, whereas data having hit signals ("1") in one data latch circuit 118_j is held in the reference current control register 118. The unit current value in each of the unit current drive circuits 66 and 74 is i_0 and the reference offset current value i_{0s} in the reference offset current drive circuit 68 is set at 0.5 i_0 on the assumption that the reference current i_r is 1.5 times as great as the unit current i_0, that is, set at 1.5 i_0.

Prior to starting the detecting operation, one data latch circuit 118_j of the reference current control register 118 is made to latch-hold the hit signal "1". With the precharge control signal line 72 set at L (low: "0"), the first and second signal lines 62 and 64, consequently contacts a and b, and further the contacts A and B within the differential current detection circuit 70 are precharged at H (high) potential (e.g., 5V) likewise.

With the precharge control signal line 72 at H (high: "1"), the PMOS transistors 78, 79, 83 are subsequently turned off and the control transistors 67d, 69d, 75d, 77d are turned on. Consequently, two NMOS transistors 75c and 75d of the unit current drive circuit 74_j and two NMOS transistors 69c and 69d of the reference offset current drive circuits 68 corresponding to one data latch circuit 118_j holding the hit signal "1" in the reference current control register 118 are simultaneously turned on. The reference current i_r (= 1.5 i_0) flows through the second signal line 64 to lower the potential of the contact a. On the other hand, the drive current i_0 flows from the first signal line through the unit current drive circuit 66_j connected to the data latch circuit 18_j whose flag data has the hit signal "1" out of m+1 of current drive circuits 66 (66_0, 66_1,..., 66_m). Since the flag data in the flag register 18 has a plurality of hit signals "1", for example, k ($k \geqq 2$) of hit signals in this case, current of ki_0 flows through the first signal line 62 and the potential of the contact a drops accordingly.

When k is greater than 2, the contact B keeps "1" because current ki_0 flowing through the first signal line 62 is greater than the reference current i_r (= 1.5 i_0) flowing through the second signal line 64 and the inverter 84 connected thereto applies "0" to the AND circuit.

The detecting operation performed by the timing control circuit 116 according to the present invention at the time the number of hit signals remaining in the flag register 18 comes up to one lowers the potential of the contact B to low level and the potential is inverted by the inverter 84, whereby "1" is applied to the AND circuit 88. The potential of the contact A is maintained at H (high) level.

When the output signal of the inverter 84 of the timing control circuit 116 changes from "0" to "1", the result of detection obtained from the AND circuit 88, that is, a switch control signal is obtained from the "1" signal and the reset signal of the flag register 18 and this switch control signal may be used to switch the flag data in the flag register 18 over to the flag data in the prefetch circuit 16.

Although the signal application transistor 67c and the normally OFF transistor 77c are provided on the side of the first signal line 62 and the signal application transistor 75c, the normally ON transistor 69c on the side of the second signal line 64, and the control transistors 67d, 75d, 69d, 77d on the grounding side in the unit current drive circuits 66, 74, the reference offset current drive circuit 68 and the dummy circuit 76 of the timing control circuit 116 of Fig. 23, the present invention is not limited to this arrangement, which may be made conversely. However, the arrangement illustrated above is preferred because, when the detecting operation is started, the ON-current directed from the first and second signal lines 62, 64 to the control transistors 67d, 77d, 75d respectively connected to the transistors 67c, 77c, 75c that have not been turned on (that have not received the hit signal "1" at the gate electrode of each) prevents the voltage of the first and second signal lines from dropping to ensure the stable operation of the differential current detection circuit 70 when the branching of the contacts A and B is started, that is, by increasing the po-

tential difference between the contacts a and b at a point of time the potential of the contacts a or b becomes lower than 3.6V.

Although the identical unit current i_0 is caused to flow through both unit current drive circuits 66 and 74, the present invention is not limited to this arrangement but different currents may be allowed to flow therethrough. At this time, the reference current i_r may be determined in accordance with the value of the reference offset current i_{0s}. Although the reference offset current i_{0s} is defined as what is smaller than the unit current i_0, the present invention is not limited to this arrangement but the current i_{0s} may be determined properly in accordance with the number of data latch circuits holding the hit signal "1" in the reference current control register 118 and the value of the reference unit current made to flow through one reference unit current drive circuit 74.

The timing control circuit 116 is basically so configured as stated above in this aspect of the present invention.

The timing control circuit 116 in this aspect of the present invention is applicable to the encoder 11 in the second aspect of the present invention. However, the present invention is not limited to this arrangement but also applicable to the circuit required to detect any given number of signals at a plurality of detection nodes.

With the semiconductor integrated circuit in the tenth aspect of the present invention as stated above in detail, the number of predetermined data in the data register for use in controlling the signal unit current drive means provided for the first signal line can be detected by making the reference current control register hold a predetermined number of data, for example, data "1" for controlling the reference unit current drive means. Therefore, the semiconductor integrated circuits according to the present invention are fit for used as timing control circuits for previously notifying or predicting the termination of the encoding operation in the encoders of content addressable memories.

Referring to Figs. 24 - 27, an encoder in the third aspect of the present invention will be described.

An encoder according to the present invention carries out match retrieval when retrieval data are fed to CAM blocks forming CAM before being transferred to a plurality of CAM subblocks. At this time, the result, that is, flag data including a signal (hit signal) matching the retrieval data is held in the plurality of CAM words on a CAM subblock basis. Then the highest priority CAM subblock is selected by a priority subblock encoder and its flag data is transferred to and held in the flag register of a priority main encoder. The priority main encoder encodes the hit signal in the flag data stored in the flag register in the order of predetermined priorities and outputs a hit address. As hit addresses are output, the hit signals in the flag register are sequentially reset in the priority main encoder.

On the other hand, a timing detection control circuit for previously notifying or predicting the termination of the hit signal detects the number of hit signals held in the flag register during the operation of encoding flag data in order to prepare to feed flag data in the second priority CAM subblock selected by the priority subblock encoder before the termination of the whole hit signal of the flag data in the first priority CAM subblock. When the number of remaining hit signals comes up to one, for example, a flag data sense circuit provided on a CAM word basis detects flag data in the second priority subblock in response to the detection signal. The flag data in the second priority CAM subblock is fed to the flag register immediately after the termination of encoding the whole hit signal in the flag data to start encoding the hit signal in the flag data. These steps are repeated to encode the hit signals in the whole CAM block, that is, to output addresses.

With the encoder according to the present invention, since the hit signal of the flag data in the CAM subblock subject to subsequent encoding has been ready to be fed to the flag register by the flag data sense (detection) circuit while the hit signal in the flag data in the preceding CAM subblock is being encoded, the time required to transfer the hit signal from the CAM subblock to the flag register of the priority main encoder can be saved. It is simultaneously detected that the number of hit signals ultimately becomes one immediately before the encoding of the last hit signal of the flat data in the flag register is started. Then the flag data sense circuit detects the flag data in the second priority CAM subblock and the flag data is fetched in the next encoding cycle so that the hit signal in the flag data thus fed can be encoded. Since no loss is caused in the encoding cycle, the encoding time in not only the whole CAM block but also the whole CAM can be shortened, whereby the high-speed match retrieval operation of CAM becomes possible.

When the number of hit signals of flag data to be encoded ultimately comes up to one while flag data in one CAM subblock is being encoded, flag data to be subsequently encoded in the CAM subblock is taken to the signal line and fetched into the flag register at the termination of the preceding encoding operation. Therefore, the flag data is encoded quickly and efficiently, and this makes not only a prefetch circuit and the like unnecessary but also the area occupied thereby reducible in the encoder according to the present invention.

Referring to the accompanying drawings, an encoder as a preferred embodiment of the present invention will be described.

Figs. 24 to 27 illustrate an encoder embodying the present invention: Fig. 24 is a block diagram including a CAM portion in the encoder according to the

present invention; Fig. 25 is a partial circuit diagram; Fig. 26 is a circuit diagram of the principal portion; and Fig. 27 is a timing chart. As the encoder 120 shown in these drawings is exactly the same in structure as the encoder 11 shown in Figs. 8 - 10 except for nothing of the prefetch circuit 16, like component elements are designated by like reference characters and the detailed description thereof will be omitted. In Fig. 24, the flag data sense circuit 126 is illustrated in a little detail, however, this configuration of the encorder 120 including the flag data sense circuit 126 is not different so great from the encoder 11 as shown in Fig. 8. Fig. 24 includes a switch circuit 124 for selecting a register 36 of a desired subblock and an AND circuit 128.

Fig. 24 is a schematic diagram of a CAM block to which the encoder in the third aspect of the present invention is applied.

The encoder 120 of Fig. 24 according to the present invention comprises a priority encoder (hereinafter called "main priority encoder" or "main encoder") 122, a priority subblock encoder (hereinafter called "subblock priority encoder" or "subblock encoder") 14, a switch circuit 124 for detecting flag data, a flag data sense circuit 126 and an AND circuit 128. The main encoder 122 comprises a flag register circuit 18, a priority circuit 20, an encode circuit 22, and a timing control circuit 60. The subblock encoder 14 comprises a latch circuit 24, a priority circuit 26, and an encode circuit 28.

As shown in Fig. 1, a CAM memory block 30 (hereinafter called "memory block") comprises a plurality (n of them B_1, B_2,..., B_n in this embodiment) of CAM subblocks (hereinafter called "subblock") 32. Further, n (A_1, A_2,..., A_n) of AND circuits 128 are provided for each subblock and there are installed m+1 (C_0, C_1,..., C_m) of flag sense circuits 126.

A description will subsequently be given of the switch circuit 124, the flag data sense circuit 126 and the AND circuit 128 for use in detecting flag data as those which best feature controlled by the present invention.

The switch circuit 124 (S_0) shown herein as a representative example which is connected to the register 36 (R_0) of the subblock 32 (B_1) comprises two NMOS transistors 124a, 124b connected in series. Each switch circuit 124 is connected to the flag data sense circuit 126 via detection lines L (L_0, L_1, ..., L_m) connected in parallel, the detection line L corresponding to the electrode (e.g., drain electrode) of one transistor 124a. The gate electrode of the transistor 124a is connected to the AND circuit 128 in parallel in each subblock 32. Moreover, the other transistor 124b is connected to the output terminal of the register 36 corresponding to its gate electrode, the electrode (e.g., source electrode) of the transistor 124b being grounded. Both transistors 124a, 124b of this switch circuit 124 are turned on when the register 36 outputs the hit signal ("1") and when a high-level signal "1" is received from the AND circuit 128 thereby, and they discharge charge by grounding the detection line L to lower the potential of the detection line L. When the data held by the register 36 is "0", the potential of the detection line L is left unchanged by the switch circuit 124 even though the high-level signal "1" is supplied from the AND circuit 128 since the transistor 124 of the switch circuit 124 remains OFF.

The flag data sense circuit 126 is formed with a self-driven type sense amplifier and precharges the detection line at a predetermined potential and detects the potential of the detection line thus precharged so as to detect the data (hit signal "1" or mismatch signal "0") held in the register 36. The flag data sense circuit 126 designated by a reference character (C_0) as what represents them by way of example is provided for the detection line L and has two PMOS transistors 126a, 126b, an inverter 126c. These flag data sense circuits 126 is such that one electrode (e.g., drain electrode) of PMOS transistor 126a or 126b is connected to the power supply, whereas the other electrode (e.g., source) is connected to the detection line L. Further, the gate of one transistor 126a is connected to the timing circuit 60 of 26 in the main encoder 122 in parallel, whereas the gate of the other transistor 126b is connected to the detection line L on the output side of the inverter 126c. The inverter 126c is indirectly connected to the detection line L and applies the inverted signal to the flag register circuit 18 of the main encoder. The flag data sense circuit 126 turns on PMOS transistors 126a, 126b while the output level (CS1) of the timing circuit 60 to be described below is low (L: "0") so as to precharge the detection line L.

Then the timing circuit 60 outputs a signal for previously notifying the termination of encoding the flag data in one subblock 32, for example, indicating that the hit signal of the flag data in the subblock being used for the encoding operation is the last one. When the output level (CS1) becomes high (H: "1"), the flag data sense circuit 126 turns off the transistor 126a and maintains the H (high) state in which the detection line L has been precharged. Incidentally, the transistor 126b is in the ON stage. On the other hand, a high-level signal (H: "1") is output from the AND circuit 128 provided in accordance with the second priority subblock 32 with "1" latched in the data latch circuit 24 of the subblock encoder 14. As a result, both transistors 124a, 124b are turned on in the word such that data in the register 36 of the selected subblock 32 is the hit signal "1" and the precharged charge is discharged from the detection line L. The potential of the detection line L is thus lowered and changed from high (H) to low (L) state. The flag data sense circuit 126 detects the potential drop of the detection line L and applies the hit signal in the register 36 to the flag register circuit 18. In other words, the inverter 126c

inverts the low (L) potential of the detection line L, turns off the PMOS transistor 126b and applies the high (H) potential hit signal "1" to the input signal line of the flag register 18 of the main encoder 122. While the output level (CS1) of the timing circuit 60 is at the high (H) level, on the other hand, the switch circuit 124 is not tuned on if the data in the register 36 of the subblock 32 is the mismatch signal "0" and the potential of the detection line L does not vary and besides the PMOS transistors 126a, 126b of the flag data sense circuit 126 are held ON. The mismatch signal "0" in the low (L) state inverted by the inverter 126c is applied from the flag data sense circuit 126 to the input signal line of the flag register 18 of the main encoder 122.

The flag data sense circuit 126 detects flag data in the second priority subblock 32 until the encoding of the last one of to-be-encoded hit signal in the flag date of the first priority subblock 32 is terminated. When the last hit signal is encoded completely before being applied to the clock terminal of the flag register 18, the flag data thus detected is immediately applied to the flag register 18 and latched therein.

The AND circuit 128 is used to AND the encode termination timing notifying signal (CS1) from the timing circuit 60 with the latch date (or rest output) in the data latch circuit of the subblock encoder 14 and to control the whole switch 124 of the corresponding subblock 32. Only when the notifying signal (CS1) and the latch data are simultaneously at H (high) level "1", the output of the AND circuit 128 is set at H (high) level and the transistor 124a in each switch circuit 124 is turned on. If the data held in the register 36 of the subblock 32 is the hit signal ("1"), the transistor 124b is turned on and the switch circuit 124 is also turned on, whereby the detection line L is grounded and the potential drops from high to low level; if, however, it is the mismatch signal ("0"), the transistor 124b is held OFF and the switch circuit 124 is not turned on and consequently the potential of the detection line L does not vary.

The main encoder 122 has the flag register circuit 18, the priority circuit 20, the encode circuit 22 and the timing circuit 60 as shown in Figs. 24 and 25. The flag register 18 has m+1 data latch parts (with reference characters attached to the corresponding detection line L for convenience) corresponding to the detection line L and these latch parts hold data on the detection line L supplied from the timing circuit according to the timing signal in the order of predetermined priorities and are reset by the signal applied from the priority circuit 20. This flag register 18 holds the flag data while the encode circuit 22 encodes all of the hit signals, and resets the hit signal at the word address each time that the hit signal at the high priority word address is encoded.

Although the flag register 18 employs a D-latch in this embodiment, any other one may be selected for use as long as one bit can be held temporarily.

The main encoder 122 of Fig. 25 for use in the encoder 120 in the third aspect of the present invention and the main encoder 12 of Fig. 12 for use in the encoder 10 in the first aspect thereof are different in that the former has the timing circuit 60 and that the node Qm (OR output) of the priority circuit 20 is not connected via the inverter 49 to the flag register 18.

More specifically, by use of termination data "0" outputted from the Q_m node after the last hit signal in the flag data held in flag registor 18 is reset, the priority circuit 20 of the main encoder 12 of Fig. 2 switch the flag data in the flag register 18 over to flag data in the second priority subblock 32 latch-held in the prefetch circuit 16. In other words, in the main encoder 12 of Fig. 2, output "0" of node Q_m is inverted by the inverter 49 and the inverted value "1" is supplied to the the flag register 18. The flag data in the next priority subblock 32 latch-held in the prefetch circuit 16 is fed to the corresponding circuit of the flag register circuit 18 and held therein. Then the flag data in the subsequent priority subblock 32 selected by the subblock encoder 14 beforehand is read from the register 36 and latch-held in the vacant prefetch circuit 16. The priority circuit 20 thus terminates the processing of the flag data in the first priority subblock and since it need not wait for the flag data in the second priority subblock transferred from the register 36 of the subblock 32, it can perform the encoding operation with efficiency likewise. In this method, however, there occurs a cycle in which the flag data in the subblock is impossible to encode when it is switched in the priority encode cycle started by resetting since the contents of the flag register 18 are switched over to the second priority flag data held in the prefetch circuit 16 after the last hit signal in the flag data in the first priority subblock held in the flag register 18 is reset. As a result, there may be produced a time interval during which no encode output operation can be performed.

In this aspect of the present invention, instead of resetting the last hit signal in the priority circuit 20 as an input signal with the result of detection (encode termination prediction signal) when the last hit signal is detected after the number of hit signals in the flag data in the flag register 18 is detected by means of the timing control circuit 60 as shown in Fig. 26, the flag data in the second priority subblock 32 held in the prefetch circuit 16 is shifted (input) to the flag register 18. With respect to even the flag data in the identical subblock, priority encoding can be carried out in the same cycle even when the flag data in the subblock is varied. Needless to say, the prefetching time (the time required to transfer the flag data from each subblock 32 to the main encoder 12) is made irrelevant to the encoding process by prefetching the flag data in the third priority subblock 32 preselected by the subblock encoder 14 from the register 36 to the pre-

fetch circuit 16 caused to have a free space by switching the flag data in the subblock of the flag register 18 according to the present invention and latch-holding the result. Encoding efficiency can thus be improved. Moreover, the last hit signal in the flag data in the flag register 18 need not be reset.

Fig. 26 shows a timing control circuit 60 which features this aspect of the present invention.

The timing control circuit 60 shown in Fig. 26 is the same in structure as what is shown in Fig. 10. In this timing control circuit 60, The output line is extended from the contact B and connected via the inverter 84 to the AND circuit 88 and its output is connected via the OR circuit 114 to the clock of each of the data latch circuit 18_0, 18_1,...18_m of the flag register 18. An initial value setting signal for setting the initial value of the flag register 18 is applied to the other input of the OR circuit 114. Moreover, the output of the inverter 84 is connected via an OR circuit 130 to the AND circuit 128 and the reset signal of the flag register 18 is applied to the other input of the AND circuit 88.

As previously noted, the timing control circuit 60 detects the number of hit signals "1" held in the flag register 18. It is apparent that more than one hit signal "1" is held in the flag register 18 if the output signal from the inverter 84 of the timing control circuit 60 is "0" and the number of hit signals is one or less if the output signal is "1". In the present invention, the CS1 signal output from the OR circuit 130 is led to the AND circuit 128 and the flag data sense circuit 126 and when the CS1 signal is "1", that is, while the remaining last one hit signal is being encoded, the reading and switching of the flag data in the memory subblock 32 is quickly performed to make the switch circuit 124, the AND circuit 128 and the flag data sense circuit 126 detect the flag data in the next memory subblock 32.

On the other hand, the subblock 32 whose block hit signal latch-held in the data latch circuit 24 is the hit signal ("1") is selected in the order of predetermined priorities, from left to right in Fig. 24, in the priority circuit 26 of the subblock encoder 14 and the priority- ordered output signal having "1" at that block address is produced. The output signal is encoded and output by the following stage encode circuit 28 before being applied to the AND circuit 128 corresponding to the subblock 128. As mentioned previously, the AND circuit 128 applies a high-level signal to the switch circuit 124 only when the block hit signal is "1" and simultaneously when the high-level signal is applied thereto from the timing circuit 60. As a result, the switch circuit 124 corresponding to the word 34 of the hit signal "1" grounds the signal line L. The flag data sense circuit 126 discharges the charge applied by the flag data sense circuit 126 to the signal line L beforehand and detects the potential drop on the signal line L, that is, the change of the potential from high to low, whereby the hit signal at the high potential inverted by the inverter 126c is applied to the flag register 18. The termination signal of the last one hit signal in the main encoder 122 causes theses hit signals (flag data) to be applied to the flag register 18.

Fig. 27 shows an encode timing chart of the main encoder 112 using the timing control circuit 60 in this aspect of the present invention in order to describe the encoding operation in the encoder by way of example.

In Fig. 27, (a) represents an encode signal indicating encode timing in the main encoder 12; (b) a reset signal indicating the reset timing of the hit signal "1" in the flag register 18; (c) a detection signal indicating detection timing at which the number of remaining hit signals in the timing control circuit 60; (d) a detection output signal (termination notifying signal) in the timing control circuit 60; (e) the signal (CS1) applied from the timing control circuit 60 via the OR circuit 130 to the AND circuit 128 and the flag data sense circuit 126; (f) a flag sense output signal (the output data signal of the flag data sense circuit 126) in the second priority subblock 32 to the flag register 18; and (g) a flag data switch control signal (termination signal) indicating shift timing of the following fag data to the flag register 18.

As is obvious from Fig. 27, while the hit signal in the same flag data held in the flag register 18 is being encoded with the predetermined priority, it has been so arranged that the encode cycle (a) and the detection cycle (c) is started (rise) after a passage of fixed time from the rise timing of the reset pulse (b) of the hit signal. When, however, the timing control circuit 60 detects the last hit signal at the detection timing activated by the encode pulse (a), the reset pulse (b) and the input pulse (g), with the detection output signal (d) as the termination notifying (prediction) signal changed from the contact B to the low level like Fig. 27(d), the CS1 signal (e) shown in Fig. 27(e) as the inverted signal of the detection output signal (d) is applied to the AND circuit 17 and the flag data sense circuit 126. Therefore, the flag data sense circuit 126 prechrages the signal line L and discharges the precharged charge by grounding the signal line L corresponding the word with the switch circuit 124 supplied with the high-level signal from the AND circuit 128. However, the potential of the signal line L corresponding to the word without the hit signal held therein does not vary and so does the precharged charge. The signal line L allows its potential to change in contrast to the flag data in the register 36, so that the output signal is settled as shown in Fig. 27(f). Fig. 27(f) illustrates the flag data having the hit signal "1" and what has no hit signal.

Then the output signal of the flag data sense circuit 126 is fetched to the flag register 18 in synchronization with the switch control signal (g) and the encoding operation is performed by the priority circuit 20 and the encode circuit 22 using the flag data in the

continuously encode cycle so that an encode address is output. The main encoder 122 thus performs the encoding operation in the predetermined cycle and produces an encode output. In this case, the switch control signal (g) is output by ANDing the reset pulse(b) and the inverted data(e) of the detection output (d).

Then the combination of the block address output from the encode circuit 28 of the subblock encoder 14 and the encoded word address from the encode circuit 22 of the main encoder 122 is sequentially output as an encoded logical address. When the final subblock 32 or the lowest priority subblock 32 is selected, further, the process concerned with the subblock encoder 14 is terminated and when the whole hit signal by the main encoder has been completed, the whole hit signal in the memory word of the whole CAM subblock is terminated to complete the match retrieval operation.

As set forth above in detail, when the match retrieval data in the CAM memory block is obtained by means of the encoder according to the present invention, the result of match retrieval in the first CAM subblock among the plurality of CAM subblocks constituting the CAM block, for example, a match signal (hit signal) matching the retrieval data in the plurality of CAM words is held in the holding means such as a register and the block hit signal indicating the presence of the CAM word matching the retrieval data is generated in the CAM subblock. On receiving a block hit signal, the priority subblock encoder subsequently selects the first priority CAM subblock and generates a subblock address. The hit signal (simultaneously over the whole word) in the first priority subblock thus selected is transferred to the priority encoder. Then the priority encoder encodes the hit signal in the order of predetermined priorities and outputs a word address. The priority subblock encoder selects the second priority CAM subblock during the encoding operation above and the switch control signal is detected by means of the data switch timing control circuit. Then, the hit signal data held by the holding means such as the register of the subblock are detected during the time up to the termination of encoding the flag data in the first priority subblock, for example, as soon as the encoding operation is terminated after the number of hit signals to be encoded becomes one, and the hit signal data are inputted in the data latch circuit of the priority encoder at the same time as the termination of encording. Accordingly, the priority encoder starts encoding the hit signal data in the second priority subblock in a continuous cycle immediately after the hit signal in the first priority subblock has been encoded completely and encodes, then, outputs the word address. Then the priority encoder combines the word address output with the subblock address output and outputs a logical address.

According to the present invention, output signals from a CAM block constituted by a plurality of CAM subblocks can be encoded efficiently at high speed without delay (switch time) at the time of subblock-to-subblock switching and output signals from a number of CAM subblocks can thus be encoded in the continuous cycle with efficiency; with the encoder according to the present invention, moreover, the area thus occupied thereby and the power consumption can also be decreased proportionally further while buffers such as prefetch circuits can be dispensed with.

Although the encoder with the prefetch circuit in the first aspect of the present invention, the semiconductor integrated circuits in the fourth to tenth aspects of the present invention, and the encoders equipped with the prefetch circuit in the second aspect of the present invention, and the encoders equipped with the flag data sense circuit in the third aspect of the present invention are basically so configured as stated above, the present invention is not limited to those arrangements above. More specifically, the timing control circuit according to the present invention is not limited to the applicable one to the encoder of a content addressable memory (CAM). Moreover, the number of hit signals to be detected is not limited to the last one and it may be greater than one. Applicable circuits may be encoders for memories such as SRAMs and DRAMs. Although the timing control circuit according to the present invention has a dummy circuit, the provision of the dummy circuit is not necessarily essential. Although the timing control circuit illustrated above is intended to detect the number of hit signals "1" held in the flag register 18, it may be designed to detect the number of signals "0". Although the timing control circuit according to the present invention detects the discharge of the signal line by the current drive means, it may conversely detect the charge up by the current drive means. In this case, the differential current detection means is intended to lower the potentials of both signal lines but detect the differential current as the potential grows.

In addition, various combinations of the semiconductor integrated circuits in these aspects of the present invention may be employed according to the present invention and they may needless to say be combined into the encoders in the versatile aspects of the present invention.

The use of the semiconductor integrated circuit according to the present invention is not limited to the manner in which it is used as a timing control circuit for the encoder but it may be used as a sense amplifier for detecting the timing variation by detecting the differential current between the currents flowing through the signal current detection line to which at least one current drive means is connected and the reference current drive line to which the reference current drive means is connected. Moreover, the semiconductor integrated circuit may be used as a

sense amplifier for reading a memory such as DRAM, SRAM and the like.

Although various aspects of the present invention have been described with reference to semiconductor integrated circuits and encoders according to the present invention by way of example, the present invention is not limited to those arrangements but may needless to say be modified in design and improved in various ways by, for example, replacing circuit elements, to say nothing of P-channel MOS transistors and N-channel MOS transistors, and changing their combinations without departing from the scope and spirit of the present invention.

Referring to Fig. 28, a dynamic sense amplifier in the eleventh aspect of the present invention will be described in detail.

Although the semiconductor integrated circuits in the fourth to tenth aspects of the present invention have been described as applications to number detection circuits for use as timing control circuits for previously notifying the timing of switching the flag data within the register of the subblock of the encoder of the memory such as CAM, SRAM, DRAM and the like, the present invention is not limited to the arrangements above but applicable to various circuits. A description will subsequently be given of a case where the present invention is applied to dynamic sense amplifiers in SRAM, DRAM, CAM and the like.

Fig. 28 illustrates various dynamic sense amplifies for use as sense amplifiers for SRAM according to the present invention. Figs. 28(a) - (f) refer to cases where the semiconductor integrated circuits shown in Figs. 10, 15, 16, 18, 19, 20 are employed and as the main component parts thereof are similar, like component elements are designated by like reference characters and the detailed description thereof will be omitted. Incidentally, Fig. 28(g) refers to a complementary sense amplifier of Fig. 28(a).

The dynamic sense amplifier 140 of Fig. 28(a) comprises a current drive type latch circuit 141 having a pair of PMOS and NMOS transistors 80a, 82a whose gates are connected to each other and a pair of PMOS and NMOS transistors 80b, 82b whose gates are connected to each other, a first and a second signal line 62, 64, each having a plurality of detection nodes, a current drive circuit 142 having serially-connected NMOS 67a, 67b provided in parallel, and serially-connected NMOS 75a, 75b provided in parallel correspondingly to a plurality of detection nodes, and a precharge circuit 143 having precharge PMOS transistors 78, 78 connected to the respective nodes $\underline{a}$ and $\underline{b}$ of the first and second signal lines 62, 64 with respect to the latch circuit 141 and the current drive circuit 142 and a PMOS transistor 79 for connecting both nodes $\underline{a}$ and $\underline{b}$.

In this case, the contact A between the serially-connected PMOS 80a and NMOS 82a in the current drive latch circuit 141 is connected to the gate connection line between PMOS 80b and NMOS 82b as a first output node $\overline{DO}$, whereas the contact B between PMOS 80b and NMOS 82b is connected to the gate connection line between PMOS 80a and MNOS 82b as a second output node DO. Moreover, the source electrodes of PMOS 80a, 80B are connected to each other and 5V, for example, which is 5V as a first supply potential.

On the other hand, the current drive circuit 142 comprises first and second current drive circuits 66, 74. Drains of the NMOS 67a and 75a for signal are respectively connected to the first and second signal lines 62, 64 and the respective gates are used as first and second input nodes, for example, for forming a pair of columns of multibit SRAM memory arrays, and connected to bit lines BL and bit bars $\overline{BL}$. Moreover, sources of NMOS 67b and 75b for control use are respectively connected to the second supply potential Vss, for example, to the grounding potential (0V), each gate of them being connected to an enable signal line (precharge signal line) 72 of the sense amplifier for inputting an enable signal OE.

In the precharge circuit 143, 83 for precharging the potential of the nodes $\underline{a}$ and $\underline{b}$, and the nodes A and B the sources of both PMOSs 78 and PMOS 83 are respectively connected to the first supply potential V_{dd}, whereas both gates thereof and the gate of PMOS 79, 83 are connected to the enable signal line 72.

The reading operation of the sense amplifier 140 will subsequently be described. First, the enable signal OE is turned to "L" at the precharge time and the control transistors 67b and 75b are held OFF, whereas both PMOSs 78, PMOS 79 and PMOSs 83 are held ON so as to precharge the first and second signal lines (nodes $\underline{a}$ and $\underline{b}$), and the contact A and B at the first supply potential (V_{dd}), for example, 5V.

In this state, there develops the potential difference between the bit line BL and the bit bar line $\overline{BL}$ in conformity with the read data in the memory cell. For example, "0" data is fed to the bit line BL and set at "L", whereas the "1" data is fed to the bit bar line $\overline{BL}$ and set at "H". When the enable signal OE becomes "H" in this case, PMOSs 78, 79 and 83 are turned off and the control transistors 67b and 75b are turned on. Consequently, current proportional to the "H" potential of the bit bar line $\overline{BL}$ applied to the gate of NMOS 75a of the second current drive circuit 74 flows through NMOS 75a and the charge precharged from the second signal line is pulled out. Since "L" potential of the bit line BL is applied to the gate of NMOS 67a of the first current drive circuit 66, on the other hand, the current proportional to the potential flows therethrough and the precharged charge is also pull out of the first signal line 62.

Although the potentials of both signal lines 62 and 64, that is, those of the nodes $\underline{a}$ and $\underline{b}$ thus drop, the potential drop at the node $\underline{b}$ is greater as the "H"

potential of the bit bar line $\overline{BL}$ is higher than the "L" potential of the bit line BL and when the potential of the contact b becomes lower than the threshold value of NMOS 82b, for example, lower than 3.6V, NMOS 82b is turned on and the potential of the contact B ultimately drops up to the ground voltage (Vss). When the potential of the contact B becomes lower than the threshold value of PMOS 80a, PMOS 80a is turned on and the potential of the contact A becomes equal to the supply potential (V_{dd}) and maintained at this level. The reading operation of the sense amplifier 140 is thus terminated.

When the "L" potential of the bit line BL is lower than the threshold value of NMOS 67a, NMOS 67a is not turned on. Consequently, only the potential of the node b drops. However, the latch circuit 141 continues to operate.

If the sense amplifier 140 of Fig. 28(a) is not provided with the precharge circuit 143, the potential difference between the nodes A and a and the potential difference between the nodes B and b remain at the threshold values of the NMOS 82a and 82b, for example, about 1.4V, so that NMOS 82a or 82b is turned on when the potentials of the nodes a and b slightly drop. As a result, the potential difference between the bit line BL and the bit bar line $\overline{BL}$ mismatches the potential difference between the nodes a and b, depending on the initial value of the current flowing through the first and second signal lines immediately after the enable signal OE is changed from "L" to "H", and the sense amplifier 140 may malfunction. Particularly when there are many detection nodes of both signal lines 62 and 64 and when the plurality of detection nodes are used for detection, the malfunction tends to occur, depending on the distance between the latch circuit 141 and the detection node. Since the precharge circuit 143 is used to raise the potentials of the nodes a and b in the sense amplifier 140 according to the present invention, the potential difference between both nodes a and b is caused to grow great enough to prevent the latch circuit 141 from malfunctioning until the potential of either node becomes lower than the threshold value of NMOS (82a or 82b). In other words, since the sense amplifier 140 according to the present invention is so arranged that the latch circuit 141 starts to operate after the potential difference between the nodes a and b becomes adequate and satisfactorily great, it has a sufficient operating margin and will never malfunction. Moreover, a sense amplifier 140A as shown in Fig. 28(h) is made of a control transistor 67e for common use as NMOSs 67b and 75b as shown in Fig. 28(a), and its operation become totally same.

Sense amplifiers 144 and 148 of Figs. 28(b) and (c) are such that gate-drain connection PMOS 145 and NMOS 149 which function as detection start level setting means are connected between the supply potential V_{dd} and a line connecting the sources of PMOS 80a and 80b. In the sense amplifiers 144 and 148 shown in Figs. 28(b) and (c), a current drive circuit employs the control transistor 67e for common use as the control transistors 67b and 75b of the current drive circuit 142 of Fig. 28(a). In these sense amplifiers 144 and 148, the operating margin is further increased by lowering the potentials of the nodes A and B relative to those of the nodes a and b using PMOS 145, NMOS 149.

A sense amplifier 150 of Fig. 28(d) is provided with detection timing control circuits 151 respectively having two serially-connected invertors 102a, 104a and 102b, 104b connected between the node a and the detection node p and between the node b and the detection node q. In this case, the threshold values of the invertors 102a and 102b are used to control the detection timing to maximize the potential difference between the nodes a and b during the operation of the latch circuit 141 in order to obtain a greater operating margin.

A sense amplifier 152 of Fig. 28(e) is provided with, in place of the detection timing control circuit 151 of Fig. 28(d), transistors 109a and 109b constituting a detection timing control circuit 153 with invertors 108a and 108b through which the gates and sources are connected. In the sense amplifier 152, the threshold values of the invertors 108a and 108b are used to control the detection timing to obtain a great operating margin.

A sense amplifier 154 of Fig. 28(f) is provided with a precharge circuit 143 in addition to the detection timing control circuit 153 of Fig. 28(e) to obtain even a greater operating margin.

A sense amplifier 156 of Fig. 28(g) is what is complementary to the sense amplifier 140 of Fig. 28(a) with the ground potential V_{ss} as the first supply potential, NMOS as the first conductive MOS transistor, PMOS as the second conductive MOS transistor, and the supply potential V_{dd} as the second supply potential.

In the latch circuit 141, the sources of NMOS 82a and 82b are connected and grounded, whereas the first and second signal lines are connected to the respective sources of PMOS 80a and 80b. A discharge circuit having discharge NMOS transistors 155 and a NMOS transistor 157 equal in potential is connected to the nodes a and b. In this case, NMOS transistors 83b are connected to the contacts A and B, and the gates of NMOSs 83b are connected to the enable signal line 72 inputting the inverted enable signal $\overline{OE}$. PMOS 158a and 158b are connected to the detection nodes p and q of the first and second signal lines, the bit line BL and the bit bar line $\overline{BL}$ being connected to the gates thereof. Moreover, PMOS 159a and 159b are connected to these PMOS 158a and 158b, the second supply potential being connected to the sources of PMOS 159a and 159b. Further, the enable signal line 72 is connected to the gates of PMOS

159a, 159b, NMOS 155, 157, an inverted enable signal $\overline{OE}$ being applied to the enable signal line 72. With this arrangement, the sense amplifier 156, like the sense amplifier 140 of Fig. 28(a), is able to operate with a great operating margin.

Unillustrated complementary sense amplifiers, like the sense amplifier 156 of Fig. 28(g), are needless to say included in the present invention.

Although the sense amplifier applied to SRAM has been described as what represents sense amplifiers in the present invention, which is not limited to these examples but may be applied to reading sense amplifiers for various memories such as DRAMs and CAMs.

Claims

1. An encoder for use in a content addressable memory having a plurality of content addressable memory subblocks, each having a plurality of content addressable memory words, the encoder comprising a priority main encoder for encoding flag data, in the order of predetermined priorities, resulting from matching with retrieval data fed to the plurality of memory words in the content addressable memory subblock, and a priority subblock encoder for assigning block-to-block priorities to the plurality of content addressable memory subblocks, the priority main encoder comprising a flag register for storing flag data to be encoded in the first priority content addressable memory subblock determined by said priority subblock encoder, and a prefetch circuit for prestoring flag data in the second priority content addressable memory subblock while the match signal in the flag register is being encoded.

2. An encoder as claimed in claim 1, further comprising means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, and means for detecting the termination of the operation of encoding the match signal in the content addressable memory subblock, wherein the match signal applied to the prefetch circuit is encoded when the detection means detects the termination of the encoding operation therein.

3. An encoder as claimed in claim 1, further comprising means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, and a . timing detection control circuit for previously detecting the termination of the operation of encoding the match signal in the flag register and switching the flag data in the flag register over to the flag data in the prefetch circuit.

4. An encoder as claimed in claim 3, wherein the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of current drive means provided in parallel to the first signal line, M of data input lines connected to the flag register and receiving M of data for respectively controlling the current drive means, a second signal line, reference current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the current drive means and current flowing through the second signal line via the reference current drive means, wherein said number detection circuit is used for detecting the number of 0 or 1 in M of the data fed from M of the data input lines.

5. An encoder as claimed in claim 4, wherein the current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

6. An encoder as claimed in claim 5, wherein he signal voltage application transistor is provided between the control transistor and the first signal line.

7. An encoder as claimed in anyone of claims 4 to 6, wherein the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

8. An encoder as claimed in anyone of claims 4 to 6, wherein the timing circuit further comprises one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

9. An encoder as claimed in anyone of claims 4 to 6, wherein the timing circuit further comprises a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

10. An encoder as claimed in claim 9, wherein the timing circuit further comprises means for precharging the respective connections between the first and second transistors and the differential current detection means.

11. An encoder as claimed in claim 3, wherein the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of unit current drive means provided in parallel to the first signal line, data registers for respectively holding M of data for controlling the unit current drive means, a second signal line, N of reference unit current drive

means provided in parallel to the second signal line, a reference current control register for holding N of data for controlling each reference unit current drive means, reference offset current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the unit current drive means and reference current flowing through the second signal line via N of the reference unit current drive means and the reference offset current drive means, wherein said number detection circuit is used for detecting the number of 0 or 1 in M of the data fed from the data register to the unit current drive means in conformity with the number of 0 or 1 in N of the data held in the reference current control register.

12. An encoder for use in a content addressable memory having a plurality of content addressable memory subblocks, each having a plurality of content addressable memory words, the encoder comprising a priority main encoder for encoding flag data, in the order of predetermined priorities, resulting from matching with retrieval data fed to the plurality of memory words in the content addressable memory subblock, and a priority subblock encoder for assigning block-to-block priorities to the plurality of content addressable memory subblocks, the priority main encoder comprising a flag register for storing flag data to be encoded in the first priority content addressable memory subblock determined by said priority subblock encoder, means for resetting match signals one after another in conformity with the operation of encoding the match signal in the content addressable memory subblock of the priority main encoder, a timing circuit for previously detecting the termination of the operation of encoding the match signal in the flag register and controlling the timing at which flag data in the second priority content addressable memory subblock is prepared, and a flag data sense circuit for detecting from the content addressable memory word the flag data in the second priority content addressable memory subblock until the termination of the operation of encoding the match signal in the flag register.

13. An encoder as claimed in claim 12, wherein the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of current drive means provided in parallel to the first signal line, M of data input lines connected to the flag register and receiving M of data for respectively controlling the current drive means, a second signal line, a reference current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the current drive means and current flowing through the second signal line via the reference current drive means, wherein said number detection circuit for detecting the number of 0 or 1 in M of the data fed from M of the data input lines.

14. An encoder as claimed in claim 13, wherein the current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

15. An encoder as claimed in claim 14, wherein the signal voltage application transistor is provided between the control transistor and the first signal line.

16. An encoder as claimed in anyone of claims 13 to 15, wherein the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

17. An encoder as claimed in anyone of claims 13 to 15, wherein the timing circuit further comprises one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

18. An encoder as claimed in anyone of claims 13 to 15, wherein the timing circuit further comprises a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

19. An encoder as claimed in claim 18, wherein the timing circuit further comprises means for precharging the respective connections between the first and second transistors and the differential current detection means.

20. An encoder as claimed in claim 12, wherein the timing circuit includes a number detection circuit comprising a first signal line, M (more than one) of unit current drive means provided in parallel to the first signal line, data registers for respectively holding M of data for controlling the unit current drive means, a second signal line, N of reference unit current drive means provided in parallel to the second signal line, a reference current control register for holding N of data for controlling each reference unit current drive means, reference offset current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the unit current drive means and reference current flowing through the second signal line via N of the reference unit current drive means and the reference offset current drive means, wherein said number detection circuit is used for detecting the number of 0 or 1 in M of the data fed from the data register to

the unit current drive means in conformity with the number of 0 or 1 in N of the data held in the reference current control register.

21. A semiconductor integrated circuit comprising a first signal line, M (one or greater) of current drive means provided in parallel to the first signal line, M of data input lines for receiving M of data for respectively controlling the current drive means, a second signal line, reference current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the current drive means and current flowing through the second signal line via the reference current drive means, wherein

said semiconductor integrated circuit is used for detecting the number of 0 or 1 in M of the data fed from M of the data input lines.

22. A semiconductor integrated circuit as claimed in claim 21, wherein the current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

23. A semiconductor integrated circuit as claimed in claim 22, wherein the signal voltage application transistor is provided between the control transistor and the first signal line.

24. A semiconductor integrated circuit as claimed in anyone of claims 21 to 23, wherein the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

25. A semiconductor integrated circuit as claimed in anyone of claims 21 to 23, further comprising one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

26. A semiconductor integrated circuit as claimed in anyone of claims 21 to 23, further comprising a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

27. A semiconductor integrated circuit as claimed in claim 26, further comprising means for precharging the respective connections between the first and second transistors and the differential current detection means.

28. A semiconductor integrated circuit comprising a first signal line, M (one or greater) of unit current drive means provided in parallel to the first signal line, data registers for respectively holding M of data for controlling the unit current drive means, a second signal line, N of reference unit current drive means provided in parallel to the second signal line, a reference current control register for holding N of data for controlling each reference unit current drive means, reference offset current drive means provided for the second signal line, and differential current detecting means for detecting the differential current between current flowing through the first signal line via M of the unit current drive means and current flowing through the second signal line via N of the reference unit current drive means and the reference offset current drive means, wherein said semiconductor integrated circuit is used for detecting the number of 0 or 1 in M of the data fed from the data register to the unit current drive means in conformity with the number of 0 or 1 in N of the data held in the reference current control register.

29. A semiconductor integrated circuit as claimed in claim 28, wherein the unit current drive means is provided with a control transistor for controlling the operating timing and a signal voltage application transistor the gate electrode of which is connected to the corresponding data input line.

30. A semiconductor integrated circuit as claimed in claim 29, wherein the signal voltage application transistor is provided between the control transistor and the first signal line.

31. A semiconductor integrated circuit as claimed in anyone of claims 28 to 30, wherein the differential current detection means is further provided with detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

32. A semiconductor integrated circuit as claimed in anyone of claims 28 to 30, further comprising one first inverter and one second inverter which are at least provided between the first and second signal lines and the differential current detection means, respectively.

33. A semiconductor integrated circuit as claimed in anyone of claims 28 to 30, further comprising a first and a second transistor which are provided between the first and second signal lines and the differential current detection means respectively, at least one first inverter provided between the gate electrode of the first transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second transistor and the second signal line.

34. A semiconductor integrated circuit as claimed in claim 33, further comprising means for precharging the respective connections between the first and second transistors and the differential current detection means.

35. A dynamic sense amplifier comprising a first and a second signal line each having at least one detection node, first and second current drive means connected to the respective nodes of the first and second signal lines and having respective first and second input nodes corresponding to these signal lines, a current drive type latch circuit for detecting the differential current between the first and second signal lines, the latch circuit having a first output node and a second output node, and means for controlling the timing detected by the current drive type latch circuit, this means being provided between the current drive type latch circuit and the detection nodes of the first and second signal lines.

36. A dynamic sense amplifier as claimed in claim 35, further comprising

a first conductive type first MOS transistor whose source is connected to a first supply potential node and whose drain is connected to the first output node, a second conductive type second transistor whose drain is connected to the first output node,

a first conductive type third MOS transistor whose source is connected to the first supply potential node and whose drain is connected to the second output node, and a second conductive type fourth transistor whose drain is connected to the second output node, wherein the gates of the first and second MOS transistors are simultaneously connected to the second output node, whereas the gates of the third and fourth MOS transistors are simultaneously connected to the first output node, wherein the source of the second MOS transistor is connected to the first signal line, whereas the source of the fourth MOS transistor is connected to the second signal line.

37. A dynamic sense amplifier as claimed in claim 36, wherein the first conductive type MOS transistor is a P- channel MOS transistor and wherein the second conductive type MOS transistor is an N-channel MOS transistor.

38. A dynamic sense amplifier as claimed in claim 36, wherein the first conductive type MOS transistor is an N- channel MOS transistor and wherein the second conductive type MOS transistor is a P-channel MOS transistor.

39. A dynamic sense amplifier as claimed in anyone of the claims 35 to 38, wherein the first current drive means comprises a first signal transistor whose one electrode is connected to the detection node of the first signal line and whose gate is made the first input node, a second signal transistor whose one electrode is connected to the detection node of the second signal line and whose gate is made the second input node, and at least one control transistor connected between the other electrodes of the first and second signal transistors and the second supply potential node to receive a control signal at its gate.

40. A dynamic sense amplifier as claimed in claim 39, wherein the at least one control transistor comprises a first control transistor connected between the first signal transistor and the second supply potential and a second control transistor connected between the second signal transistor and the second supply potential.

41. A dynamic sense amplifier as claimed in claim 39, wherein the at least one control transistor is a transistor to be connected between the mutual source connection of the first and second signal transistors and the second supply potential.

42. A dynamic sense amplifier as claimed in anyone of claims 35 to 41, wherein the detection timing control means is node potential setting means for setting the respective nodes of the first and second signal lines at a predetermined potential.

43. A dynamic sense amplifier as claimed in claim 42, wherein the node potential setting means is precharge means.

44. A dynamic sense amplifier as claimed in claim 42 or 43, further comprising detection start level setting means for securing a relatively great difference between detection start voltage and the identical voltage preset to the first and second signal lines.

45. A dynamic sense amplifier as claimed in claim 44, wherein the detection start level setting means is a first conductive type MOS transistor or a second conductive type MOS transistor provided between the current drive type latch circuit and the first supply potential node.

46. A dynamic sense amplifier as claimed in claims 35 to 43, wherein the detection timing control means comprises a first and a second switch transistor, at least one first inverter provided between the gate electrode of the first switch transistor and the first signal line, and at least one second inverter provided between the gate electrode of the second switch transistor and the second signal line.

47 A dynamic sense amplifier as claimed in claims 35 to 41, wherein the detection timing control means is at least one inverter.

FIG. 1

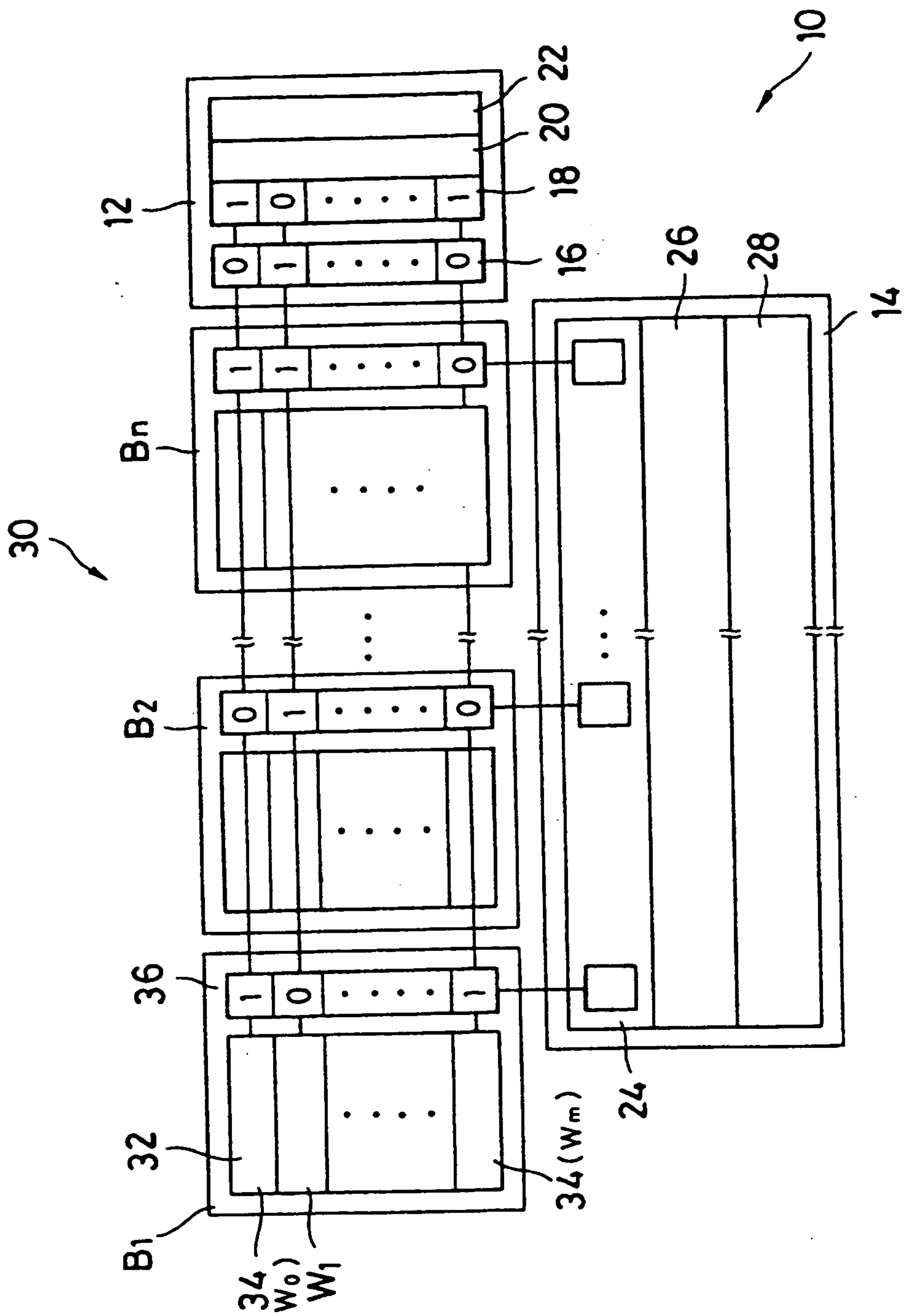


FIG. 2

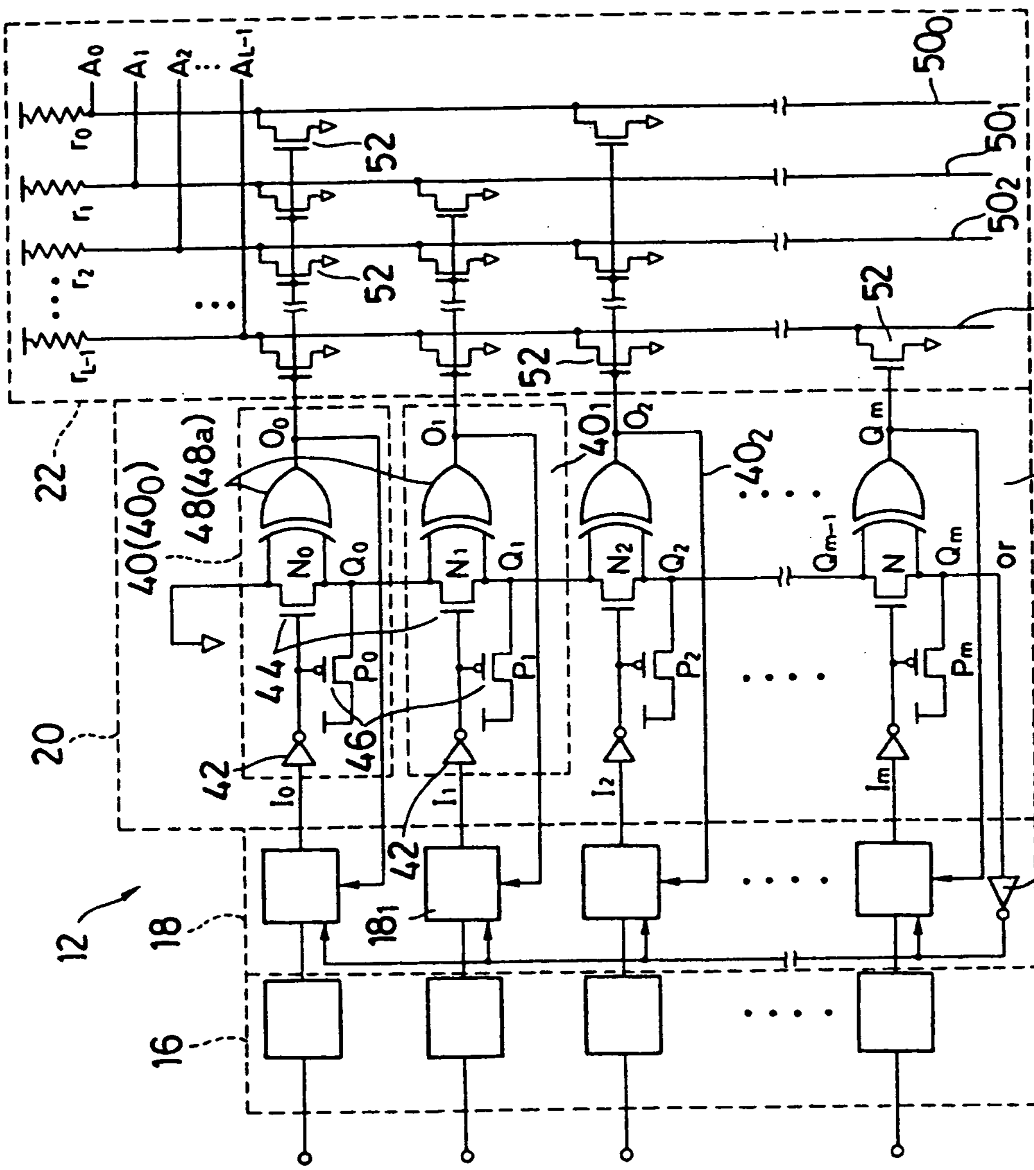

12
16
18
18_1
20
22
$40(40_0)$
40_1
40_2
40_m
42
44
46
$48(48a)$
49
52
50_0
50_1
50_2
50_{L-1}
A_0
A_1
A_2
A_{L-1}
r_0
r_1
r_2
r_{L-1}
O_0
O_1
O_2
Q_m
N_0
N_1
N_2
N
Q_0
Q_1
Q_2
Q_{m-1}
P_0
P_1
P_2
P_m
I_0
I_1
I_2
I_m
or

FIG. 3

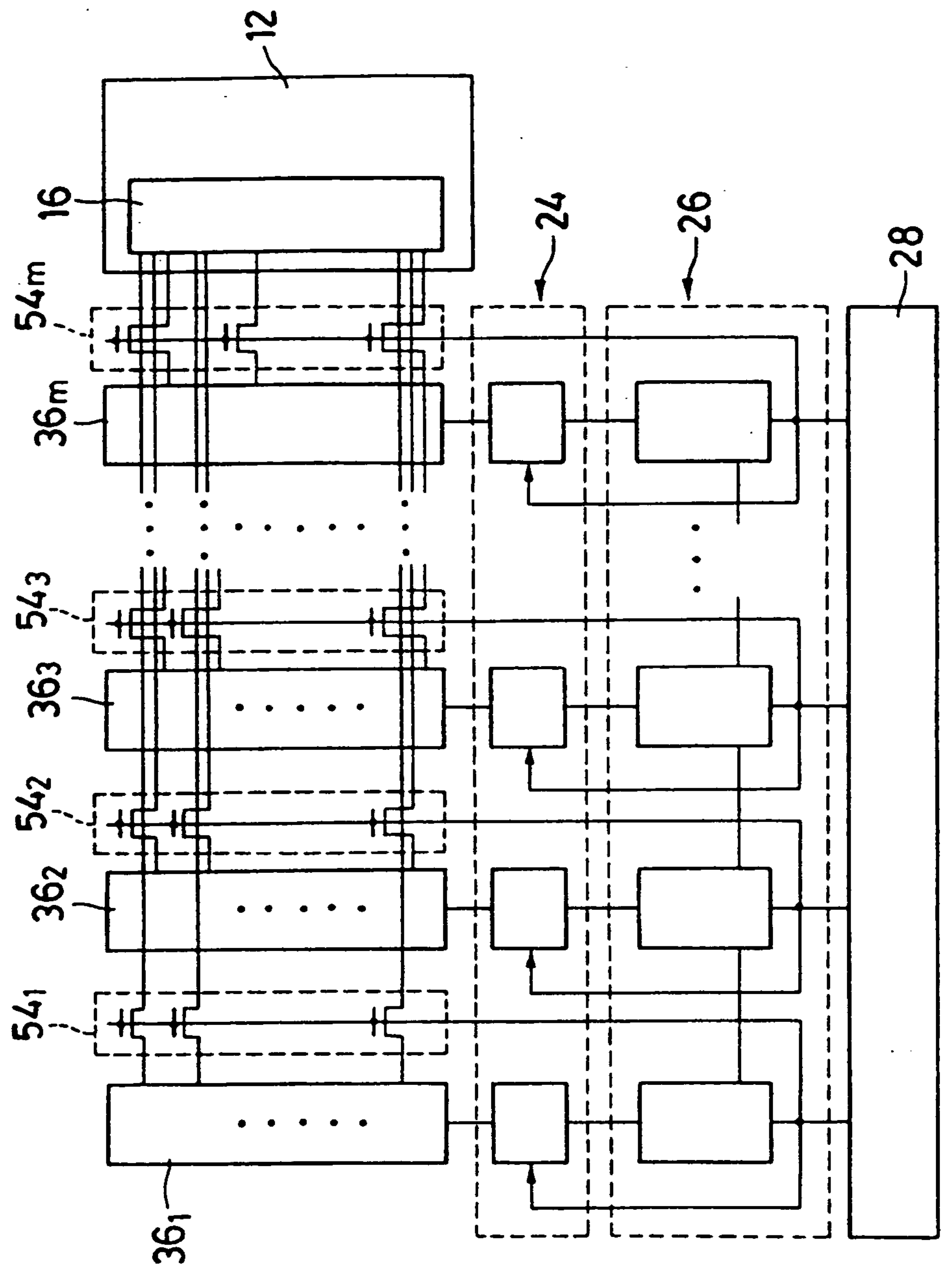
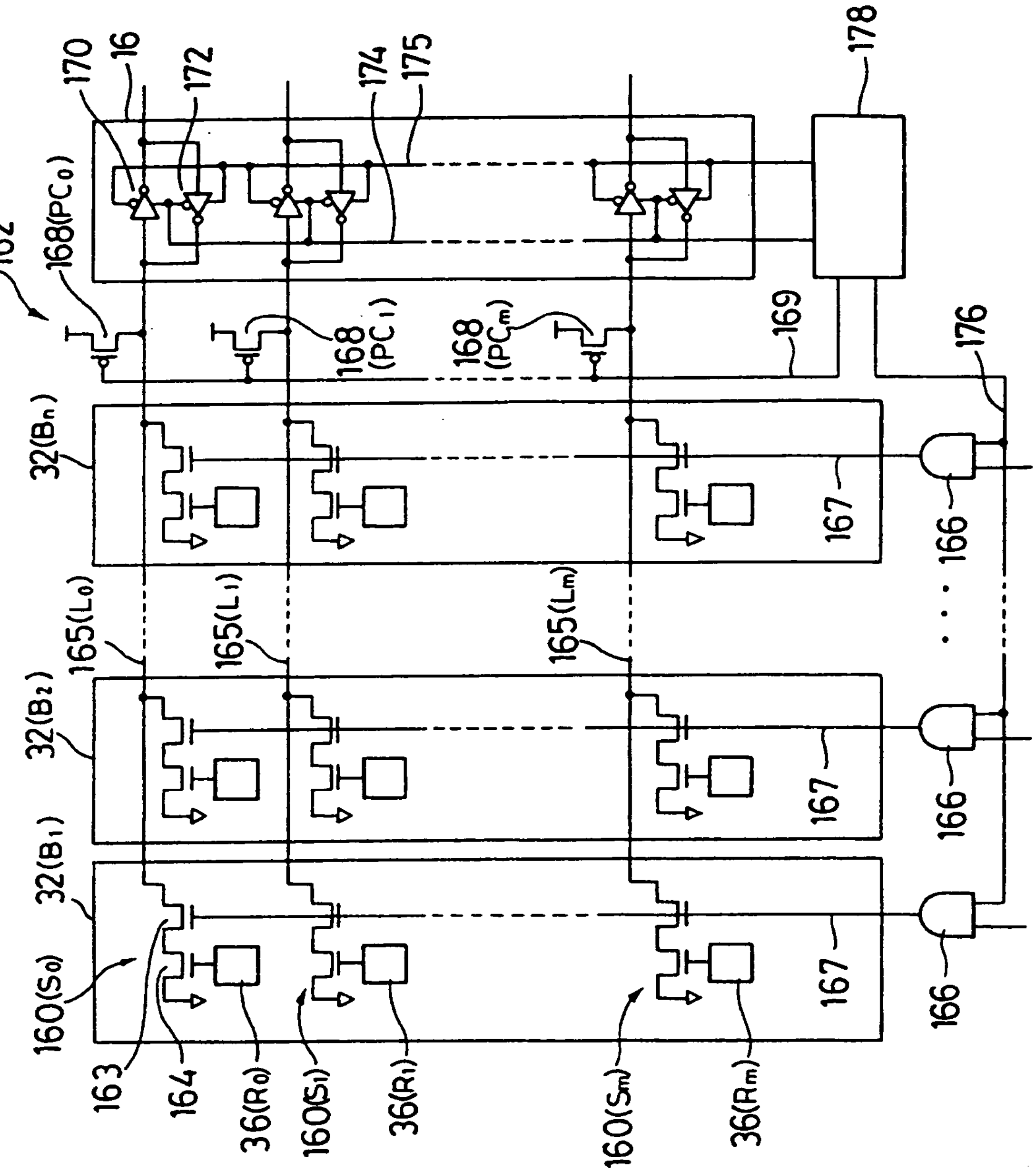
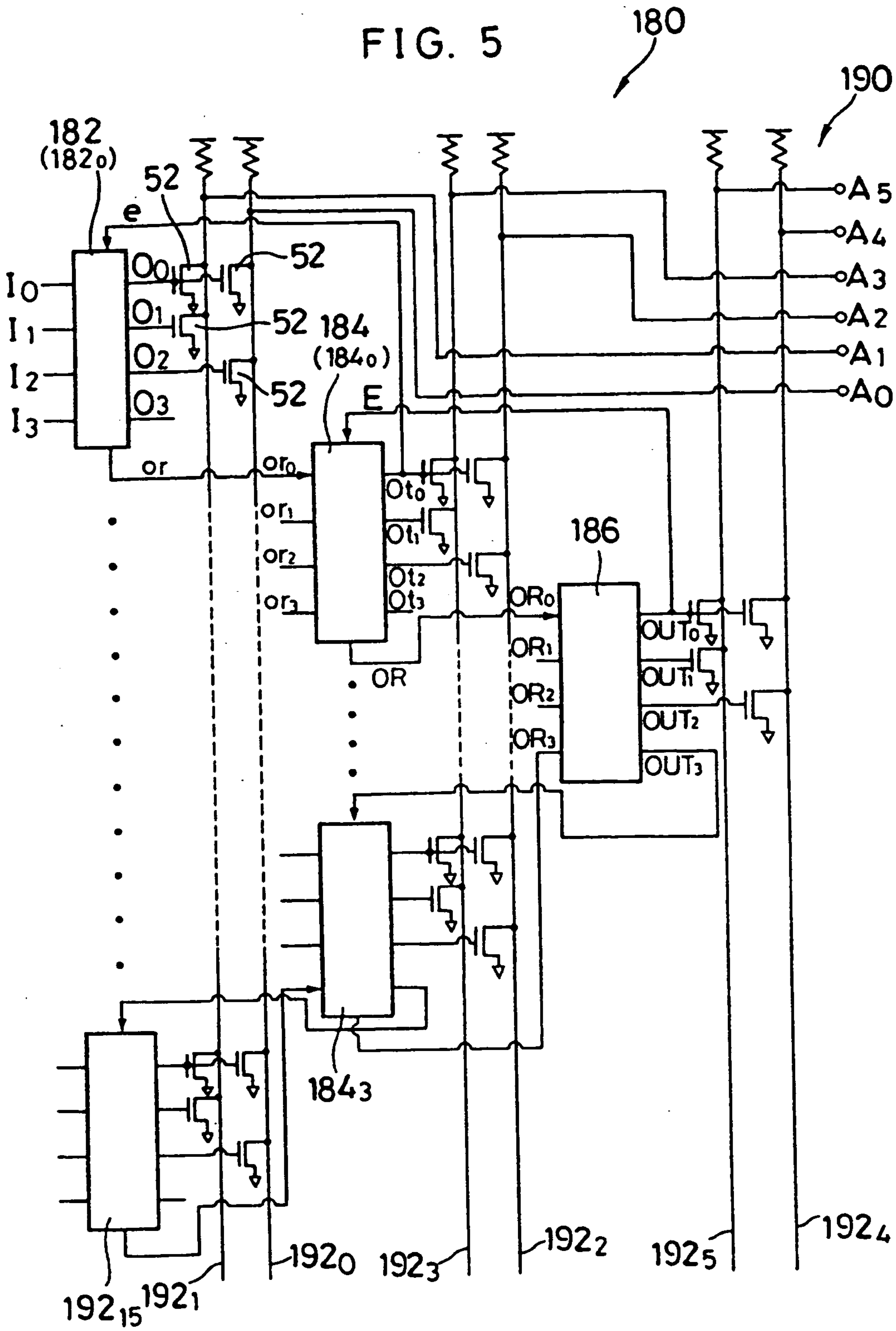


FIG. 4



162
168(PC₀)
170
16
172
174
175
178
168 (PC₁)
168 (PCₘ)
169
176
32(Bₙ)
32(B₂)
32(B₁)
165(L₀)
165(L₁)
165(Lₘ)
160(S₀)
163
164
36(R₀)
160(S₁)
36(R₁)
160(Sₘ)
36(Rₘ)
167
166

FIG. 5



180
190
182
(182o)
52
e
O0
O1
O2
O3
I0
I1
I2
I3
52
52
52
184
(184o)
E
or
or0
or1
or2
or3
Ot0
Ot1
Ot2
Ot3
OR
186
OR0
OR1
OR2
OR3
OUT0
OUT1
OUT2
OUT3
A5
A4
A3
A2
A1
A0
1843
19215
1921
1920
1923
1922
1925
1924

FIG. 6

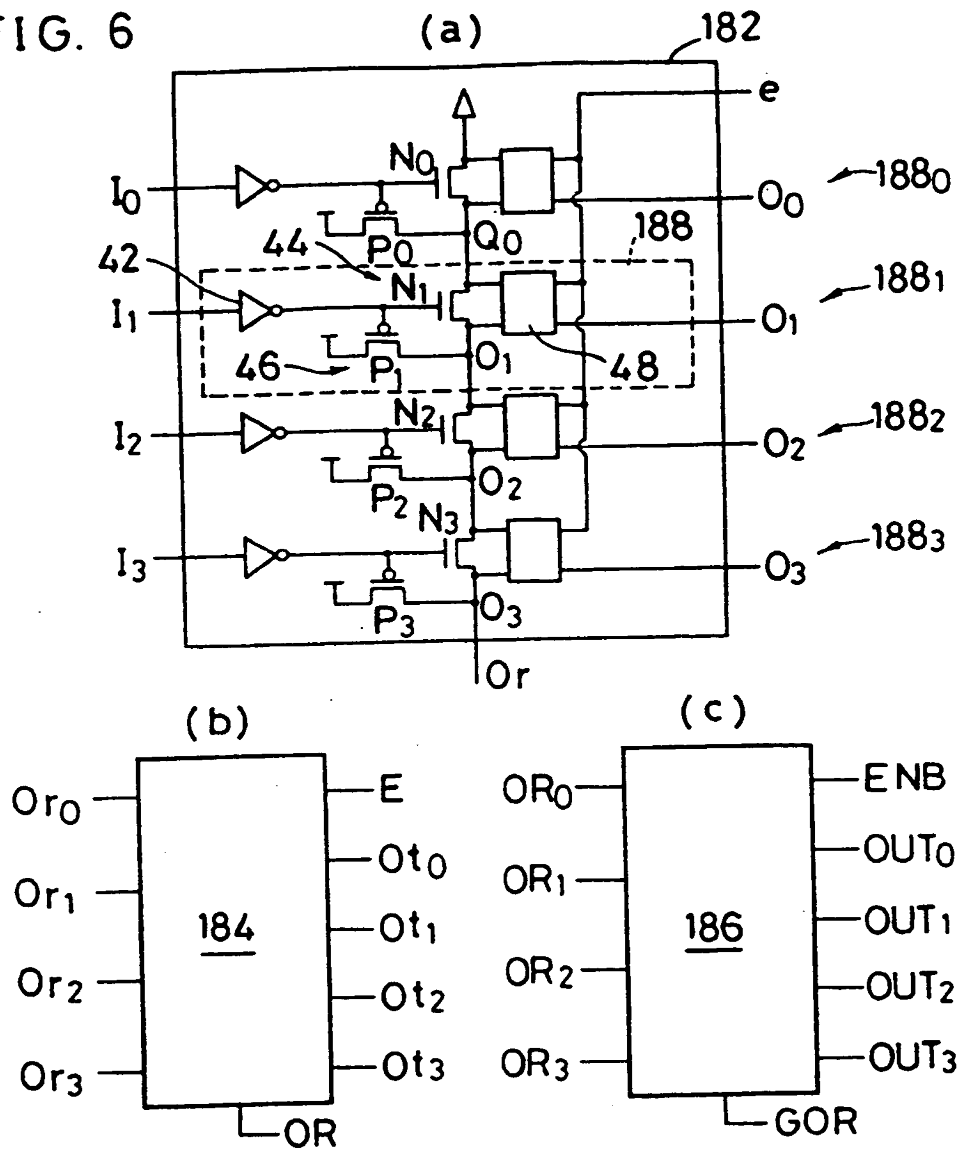

(a)
182
e
I_0
N_0
O_0
188_0
Q_0
P_0
44
188
42
N_1
I_1
O_1
188_1
46
P_1
O_1
48
N_2
I_2
O_2
188_2
O_2
P_2
N_3
I_3
O_3
188_3
P_3
O_3
Or
(b)
Or_0
E
Ot_0
Or_1
184
Ot_1
Or_2
Ot_2
Or_3
Ot_3
OR
(c)
OR_0
ENB
OUT_0
OR_1
186
OUT_1
OR_2
OUT_2
OR_3
OUT_3
GOR

FIG. 7

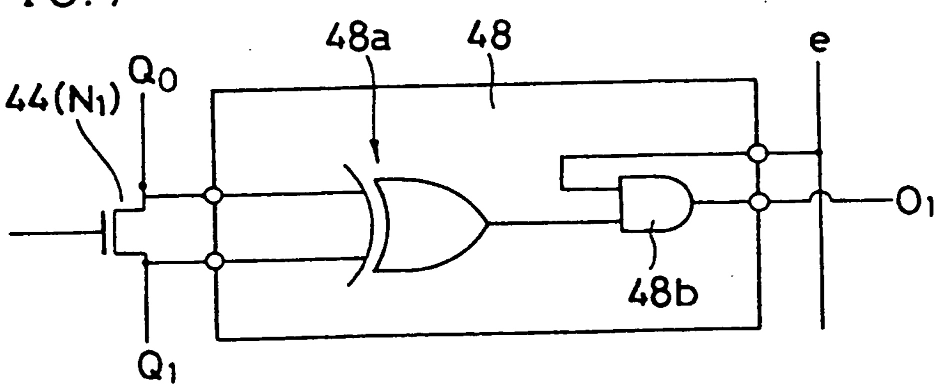

48a
48
e
44(N_1)
Q_0
O_1
48b
Q_1

FIG. 8

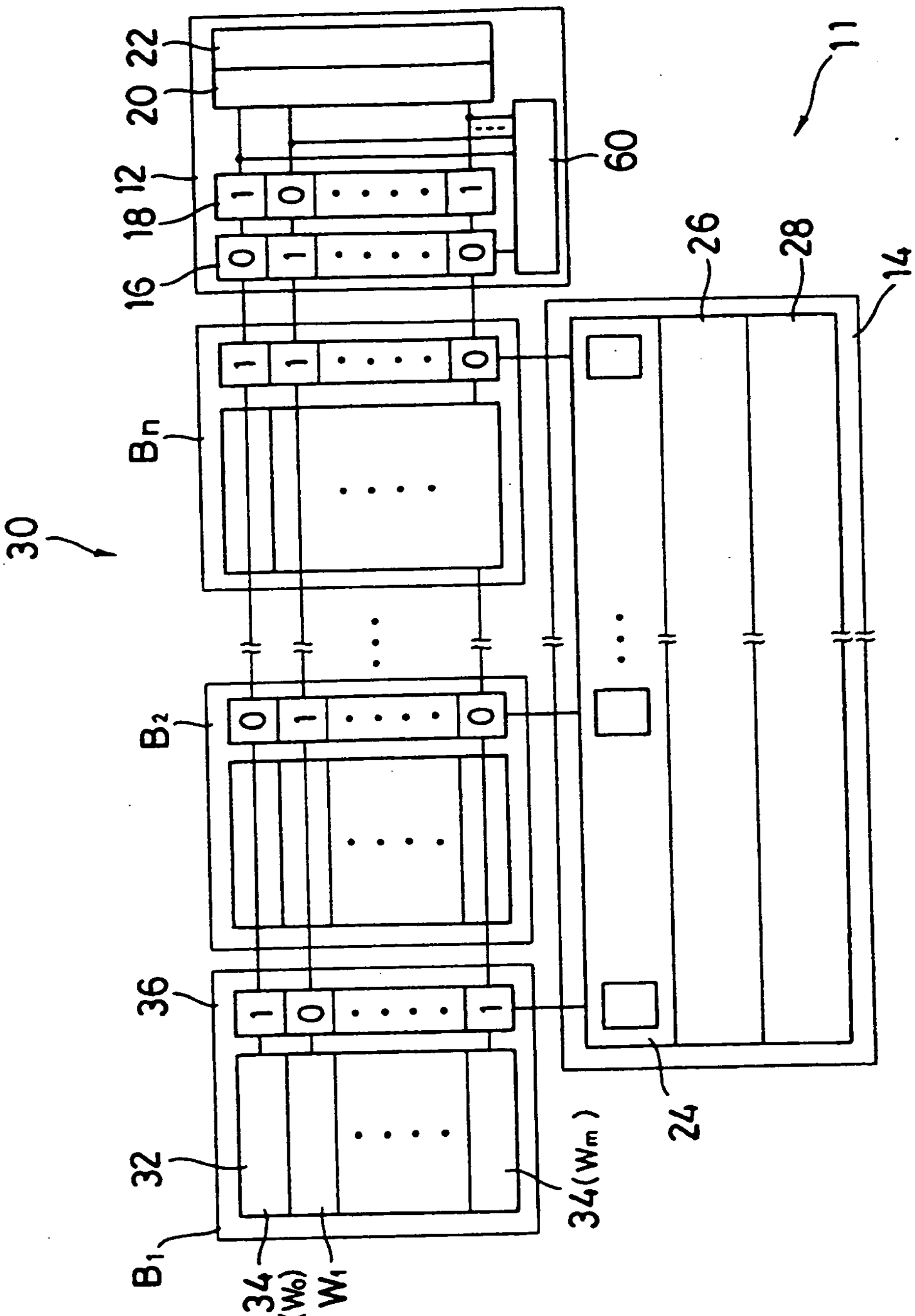


FIG. 9

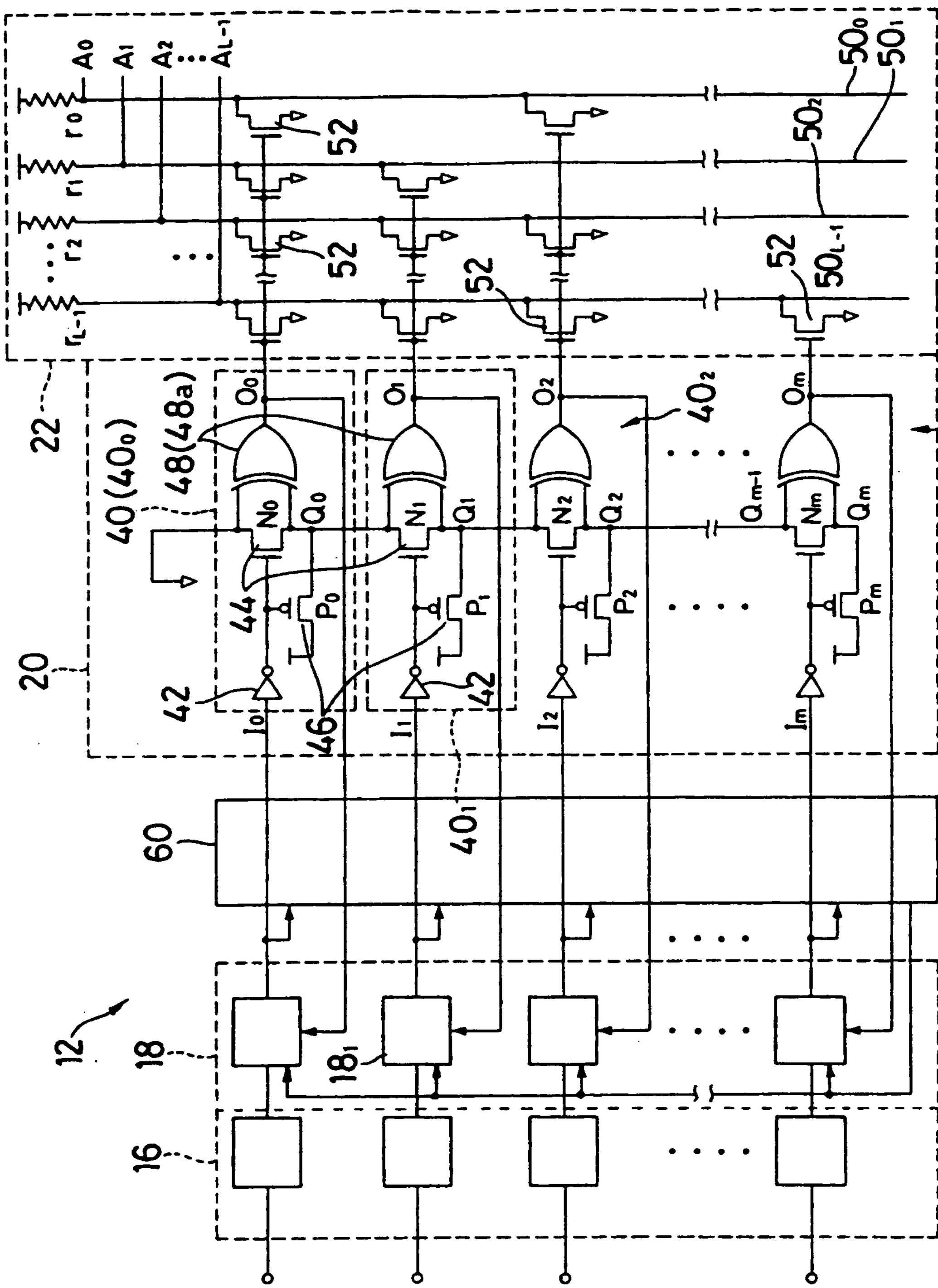

12
16
18
18₁
60
20
22
40(40₀)
40₁
40₂
40m
42
44
46
48(48a)
52
50₀
50₁
50₂
50L-1
A0
A1
A2
AL-1
r0
r1
r2
rL-1
N0
N1
N2
Nm
Q0
Q1
Q2
Qm-1
Qm
P0
P1
P2
Pm
O0
O1
O2
Om
I0
I1
I2
Im

FIG.10

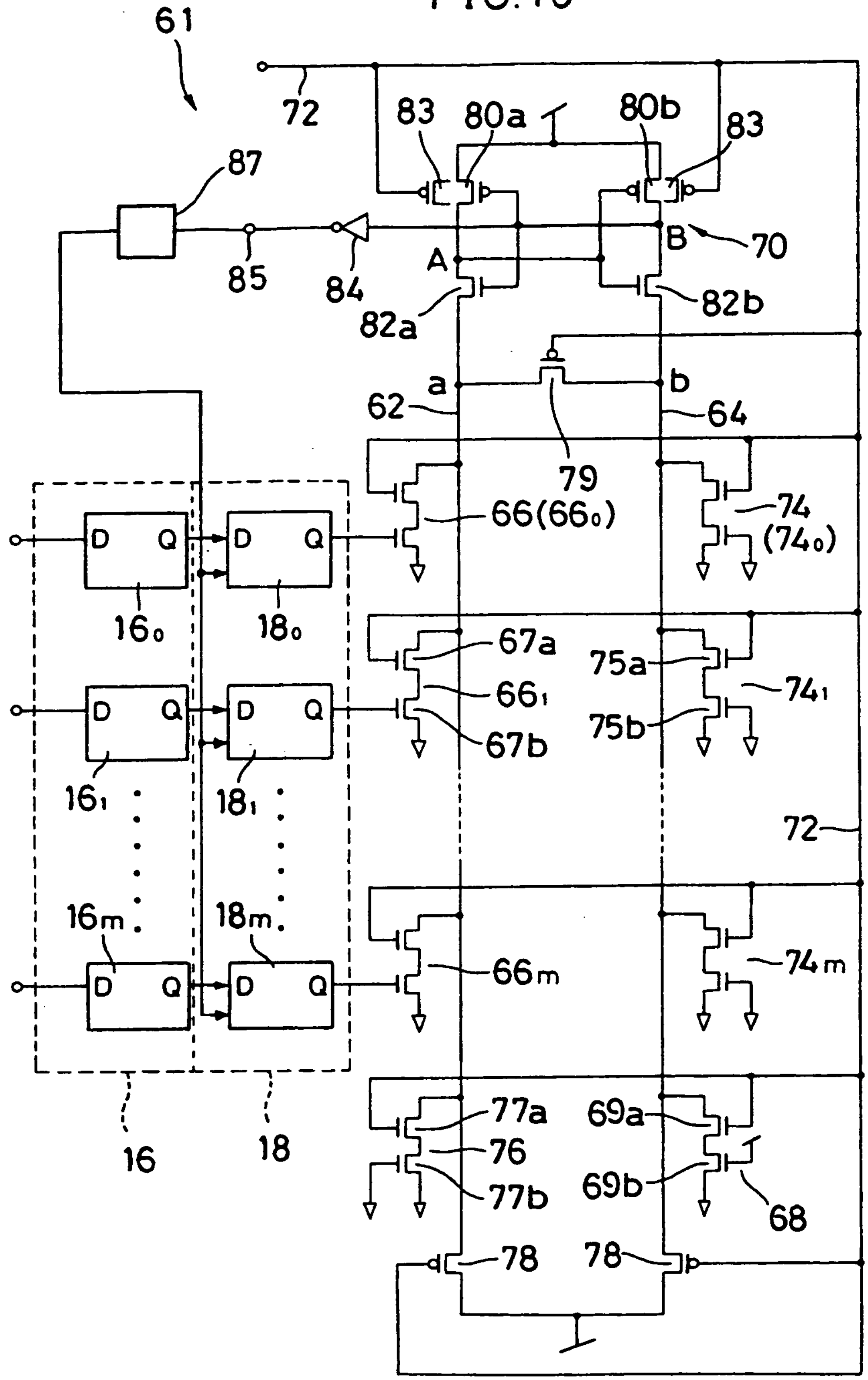

61
72
83
80a
80b
83
87
85
84
B
70
A
82a
82b
a
b
62
64
79
D Q
16₀
18₀
66(66₀)
74
(74₀)
67a
66₁
67b
75a
74₁
75b
16₁
18₁
72
16m
18m
66m
74m
16
18
77a
76
77b
69a
69b
68
78
78

FIG. 11

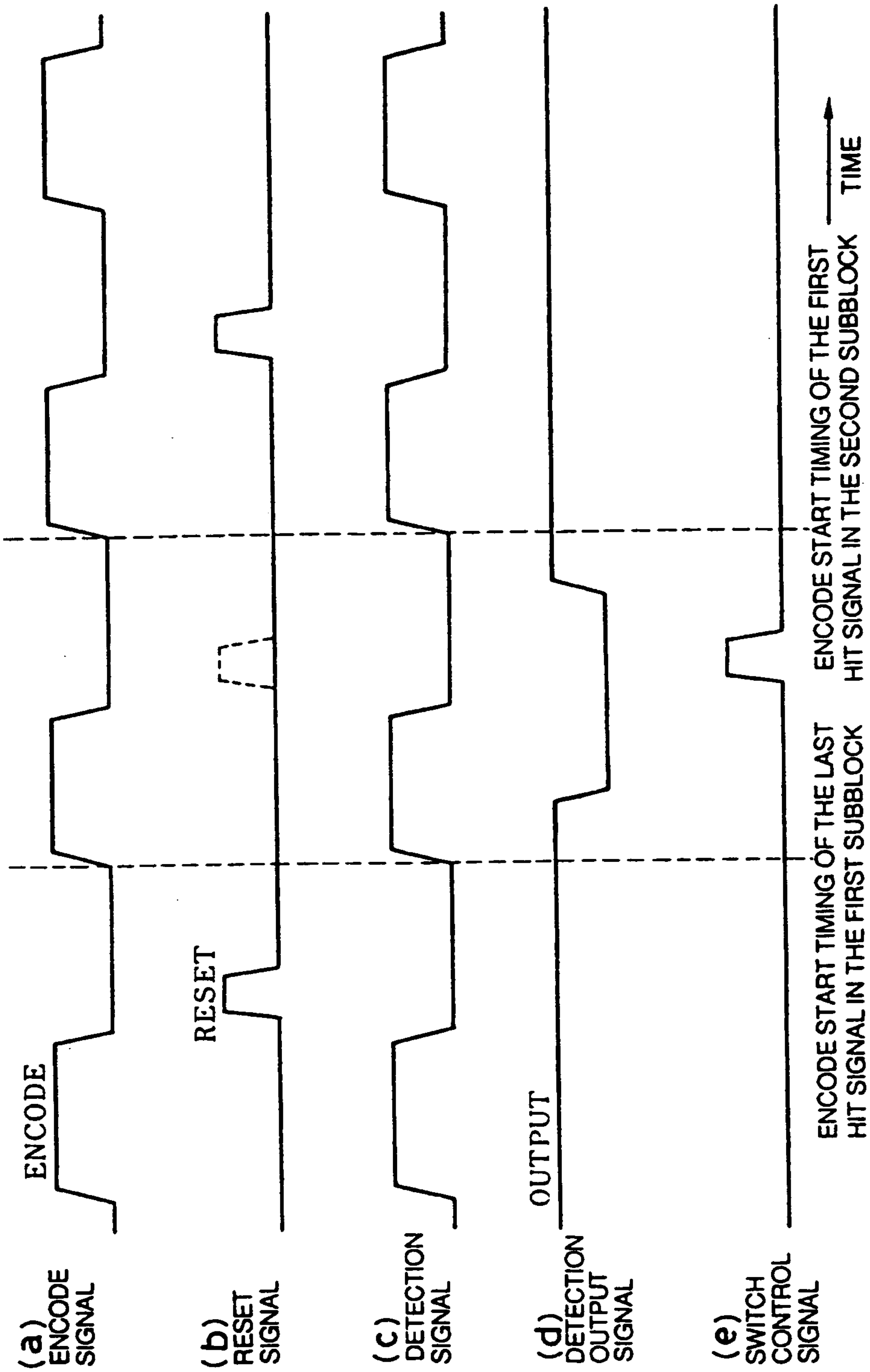

(a) ENCODE SIGNAL
(b) RESET SIGNAL
(c) DETECTION SIGNAL
(d) DETECTION OUTPUT SIGNAL
(e) SWITCH CONTROL SIGNAL
ENCODE
RESET
OUTPUT
ENCODE START TIMING OF THE LAST HIT SIGNAL IN THE FIRST SUBBLOCK
ENCODE START TIMING OF THE FIRST HIT SIGNAL IN THE SECOND SUBBLOCK
TIME

FIG. 12

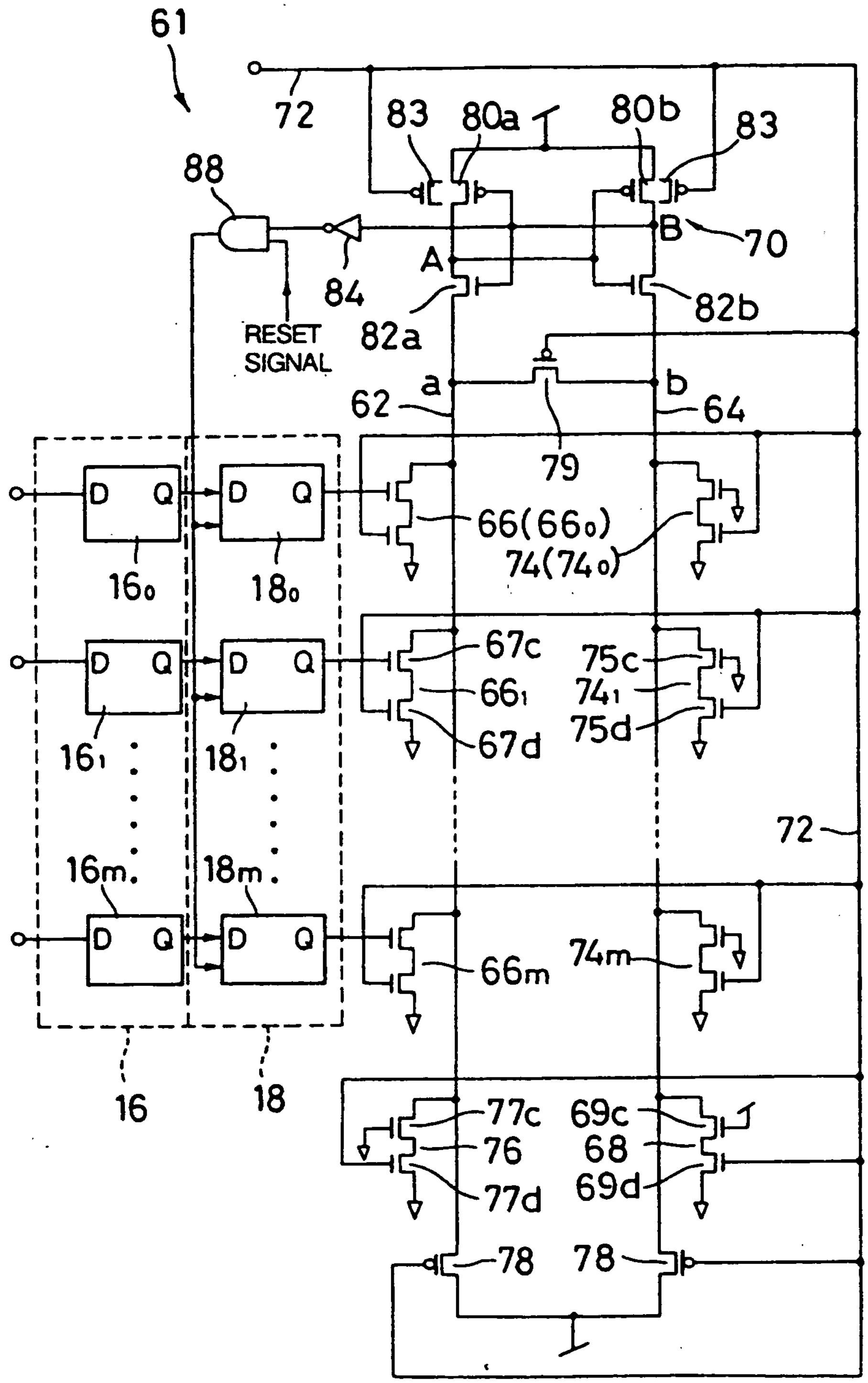
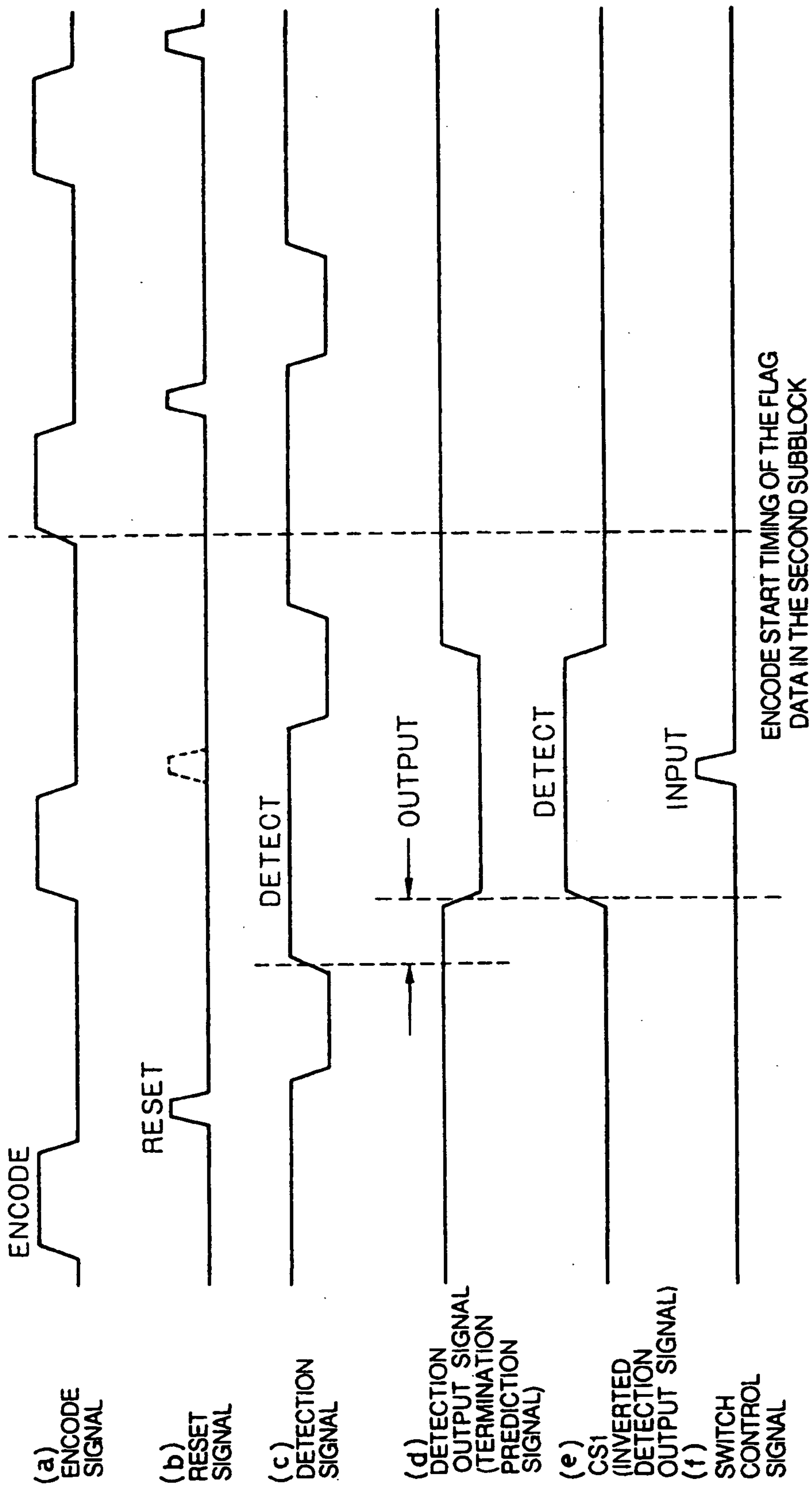

61
72
83
80a
80b
83
88
B
70
A
84
82a
82b
RESET SIGNAL
a
b
62
64
79
D Q
D Q
66(66₀)
74(74₀)
16₀
18₀
67c
75c
66₁
74₁
67d
75d
16₁
18₁
72
16m
18m
66m
74m
16
18
77c
69c
76
68
77d
69d
78
78

FIG.13


(a) ENCODE SIGNAL
(b) RESET SIGNAL
(c) DETECTION SIGNAL
(d) DETECTION OUTPUT SIGNAL (TERMINATION PREDICTION SIGNAL)
(e) CS1 (INVERTED DETECTION OUTPUT SIGNAL)
(f) SWITCH CONTROL SIGNAL
ENCODE
RESET
DETECT
OUTPUT
DETECT
INPUT
ENCODE START TIMING OF THE FLAG DATA IN THE SECOND SUBBLOCK

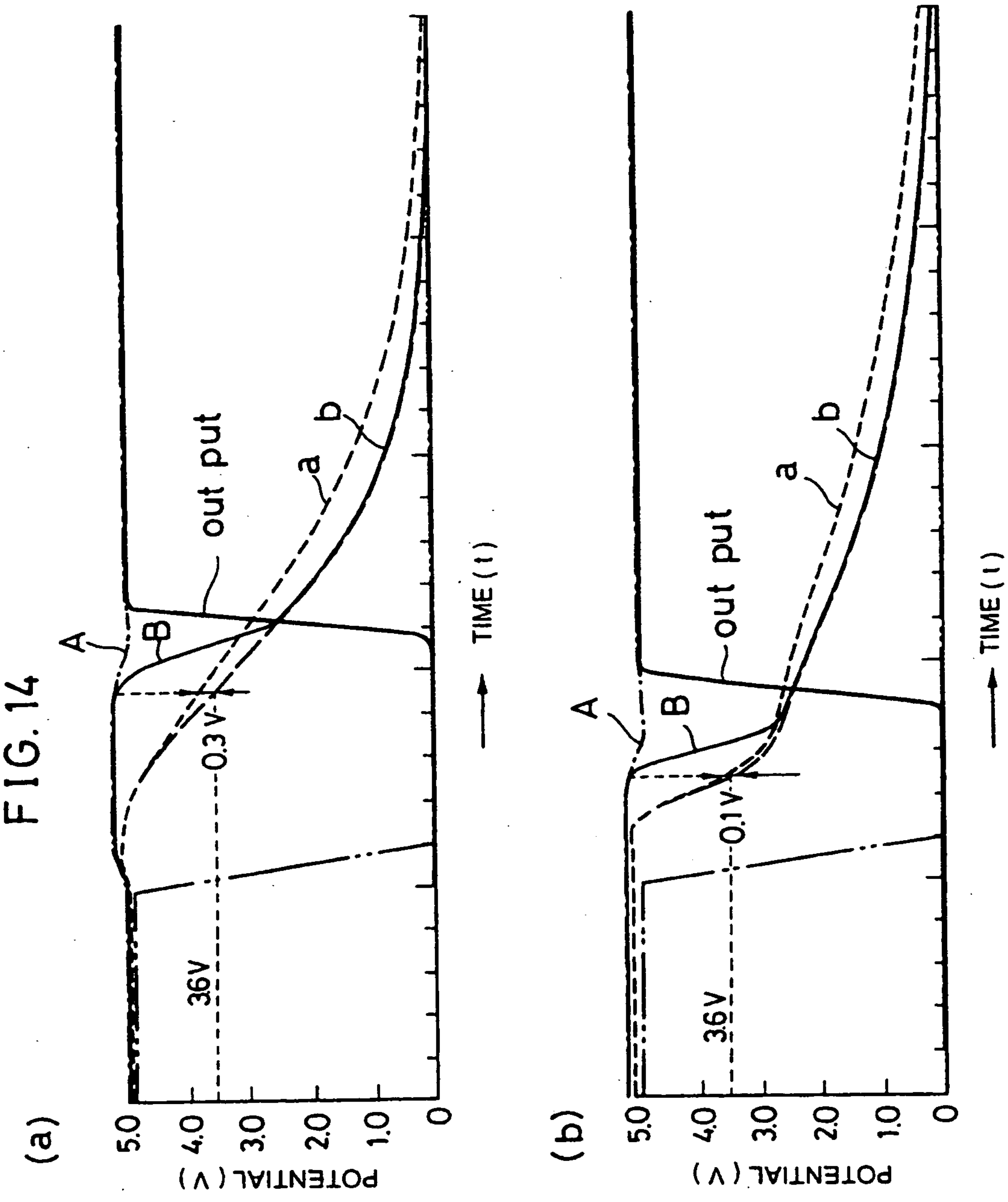

(a)
POTENTIAL (V)
5.0
4.0
3.0
2.0
1.0
0
36V
0.3 V
A
B
out put
a
b
TIME (t)
(b)
POTENTIAL (V)
5.0
4.0
3.0
2.0
1.0
0
36V
0.1 V
A
B
out put
a
b
TIME (t)

FIG. 14

FIG. 15

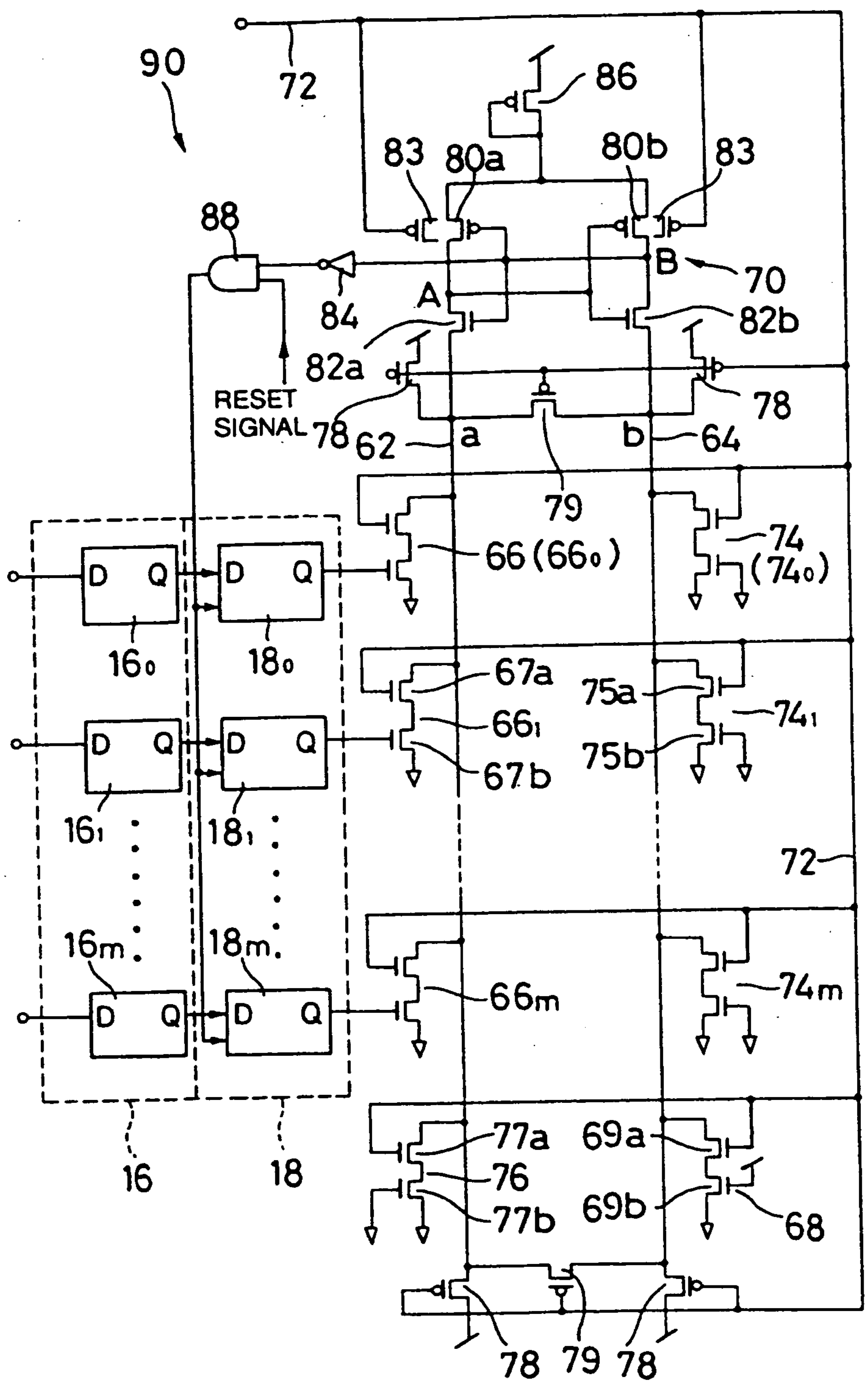

90
72
86
83
80a
80b
83
88
B
70
84
A
82b
82a
RESET SIGNAL
78
78
62
a
b
64
79
D Q
D Q
66 (66₀)
74 (74₀)
16₀
18₀
67a
75a
66₁
74₁
D Q
D Q
67b
75b
16₁
18₁
72
16m
18m
D Q
D Q
66m
74m
77a
69a
76
77b
69b
68
16
18
78
79
78

FIG. 16

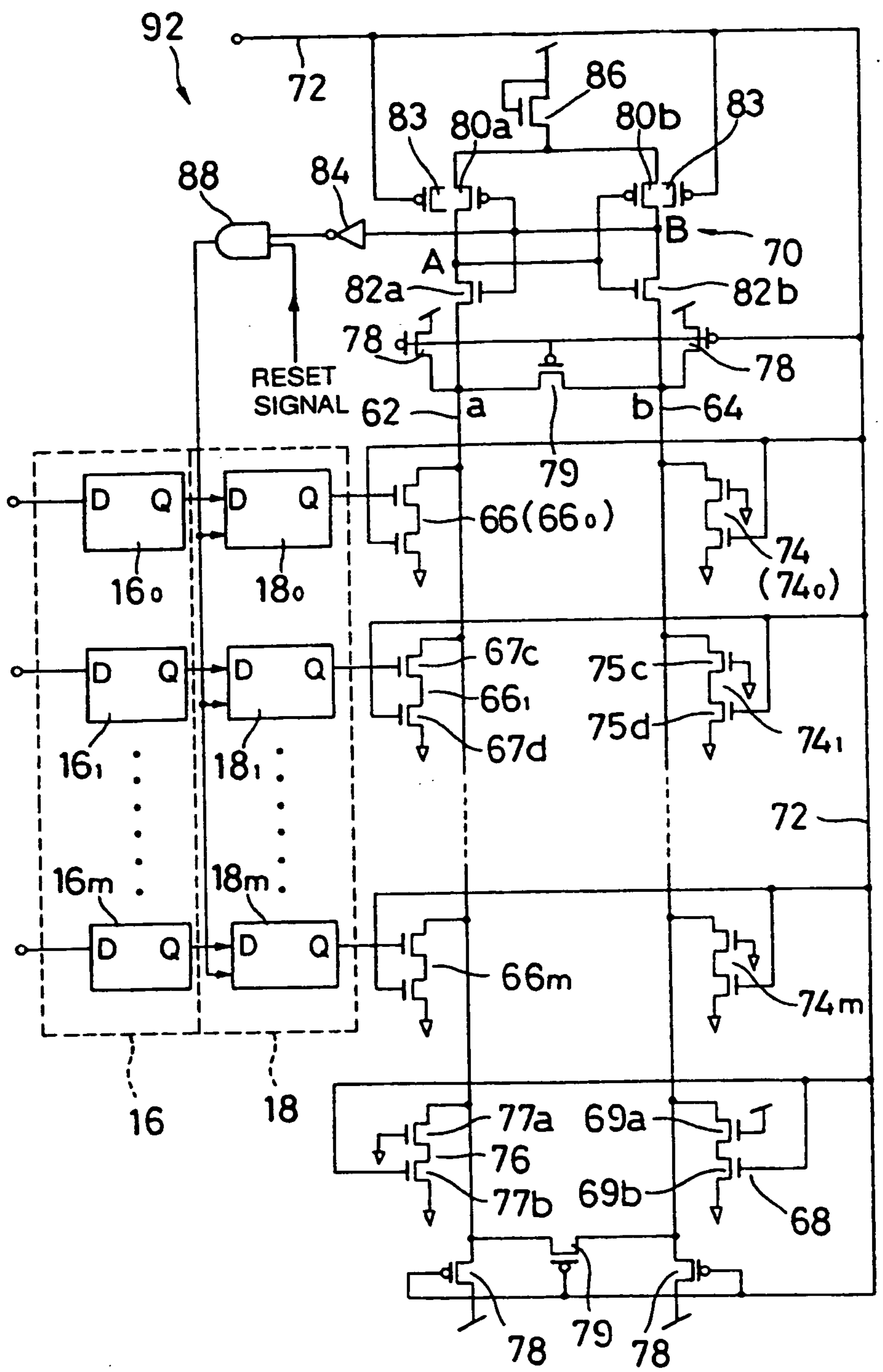

92
72
86
83
80a
80b
83
88
84
B
70
A
82a
82b
78
78
RESET
SIGNAL
62
a
b
64
79
D Q
D Q
66(66₀)
74
(74₀)
16₀
18₀
D Q
D Q
67c
75c
66₁
67d
75d
74₁
16₁
18₁
72
16m
18m
D Q
D Q
66m
74m
16
18
77a
69a
76
77b
69b
68
78
79
78

FIG.17

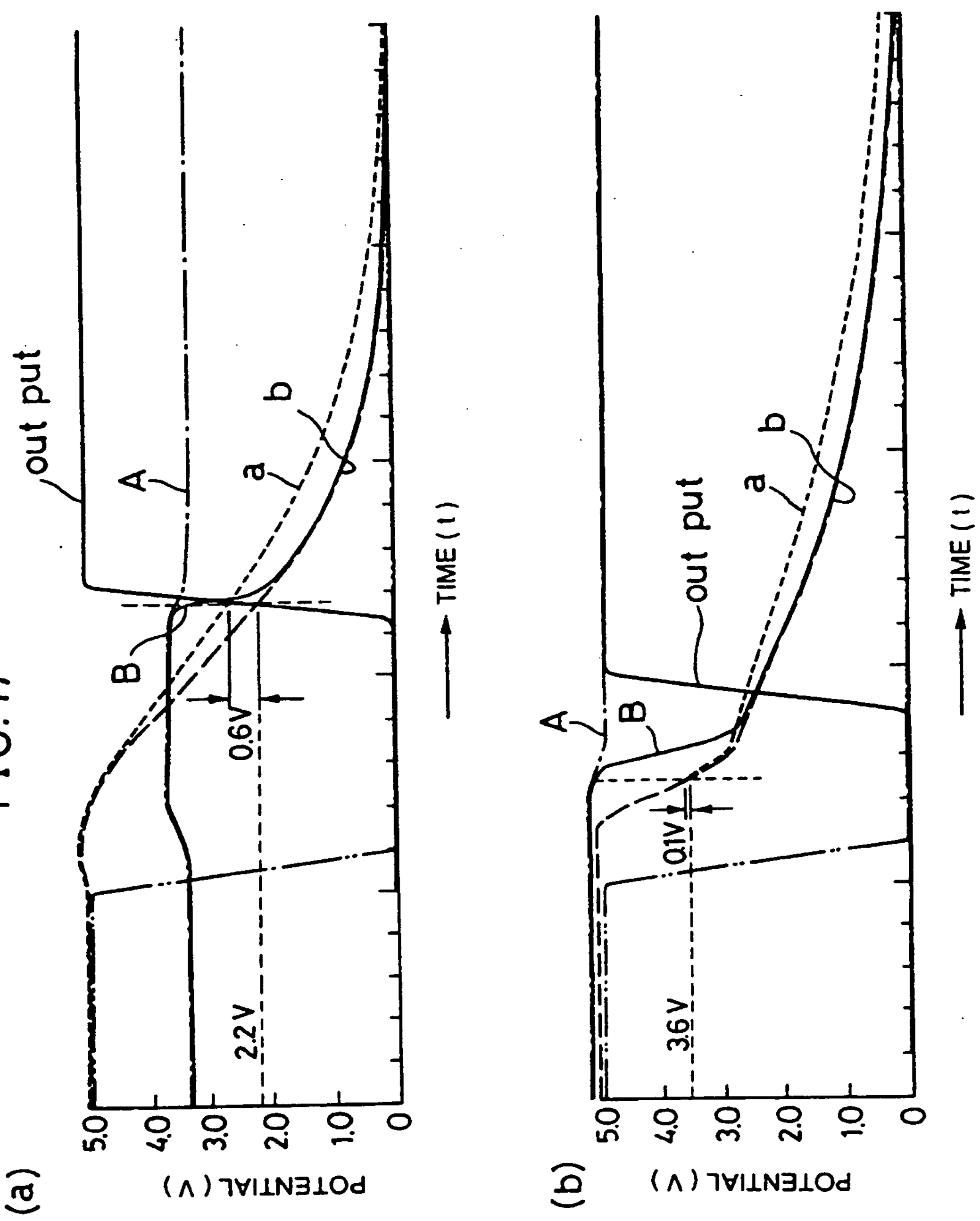

(a)
POTENTIAL (V)
5.0
4.0
3.0
2.0
1.0
0
out put
A
B
a
b
0.6V
2.2V
TIME (t)
(b)
POTENTIAL (V)
5.0
4.0
3.0
2.0
1.0
0
out put
A
B
a
b
0.1V
3.6V
TIME (t)

FIG. 18

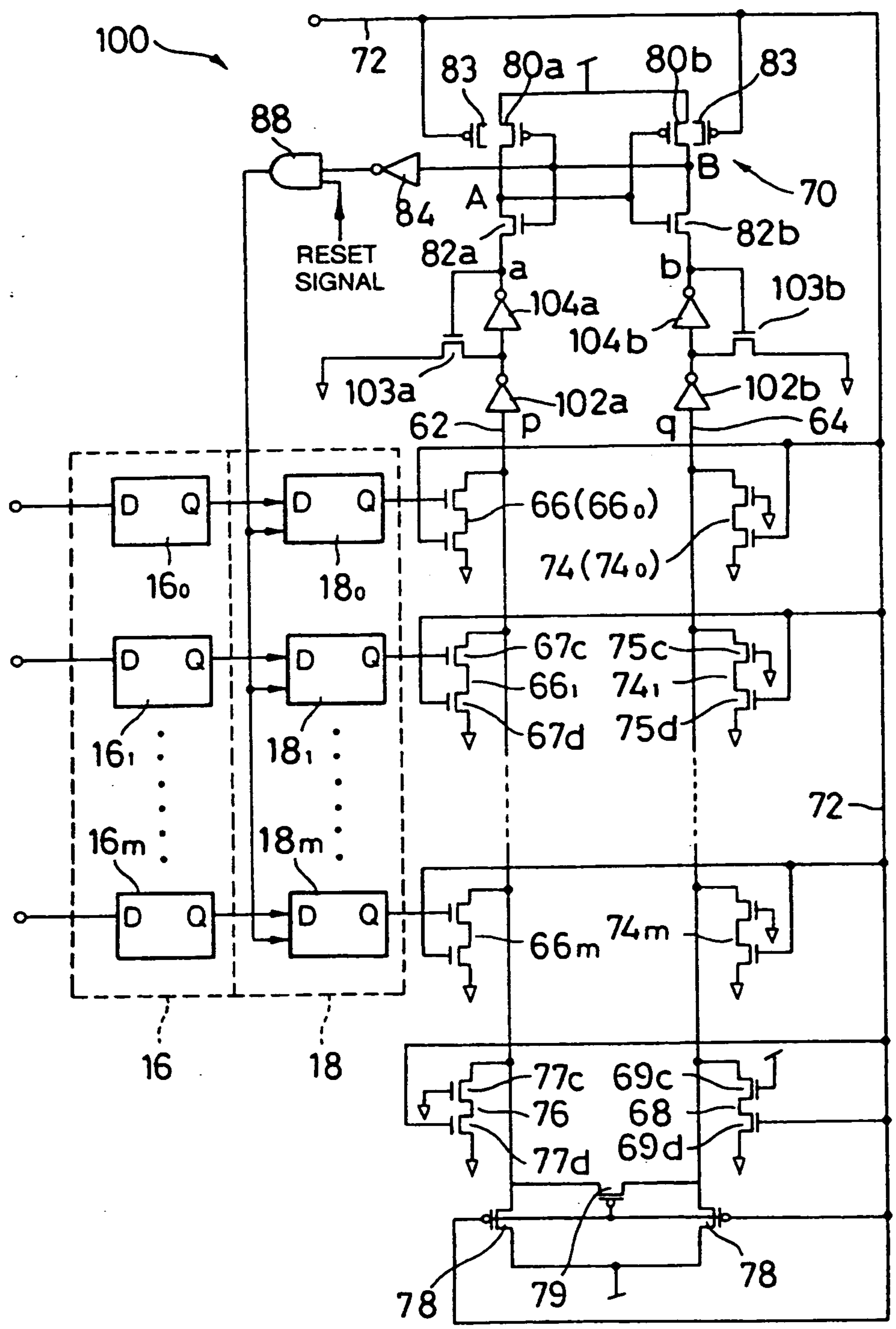
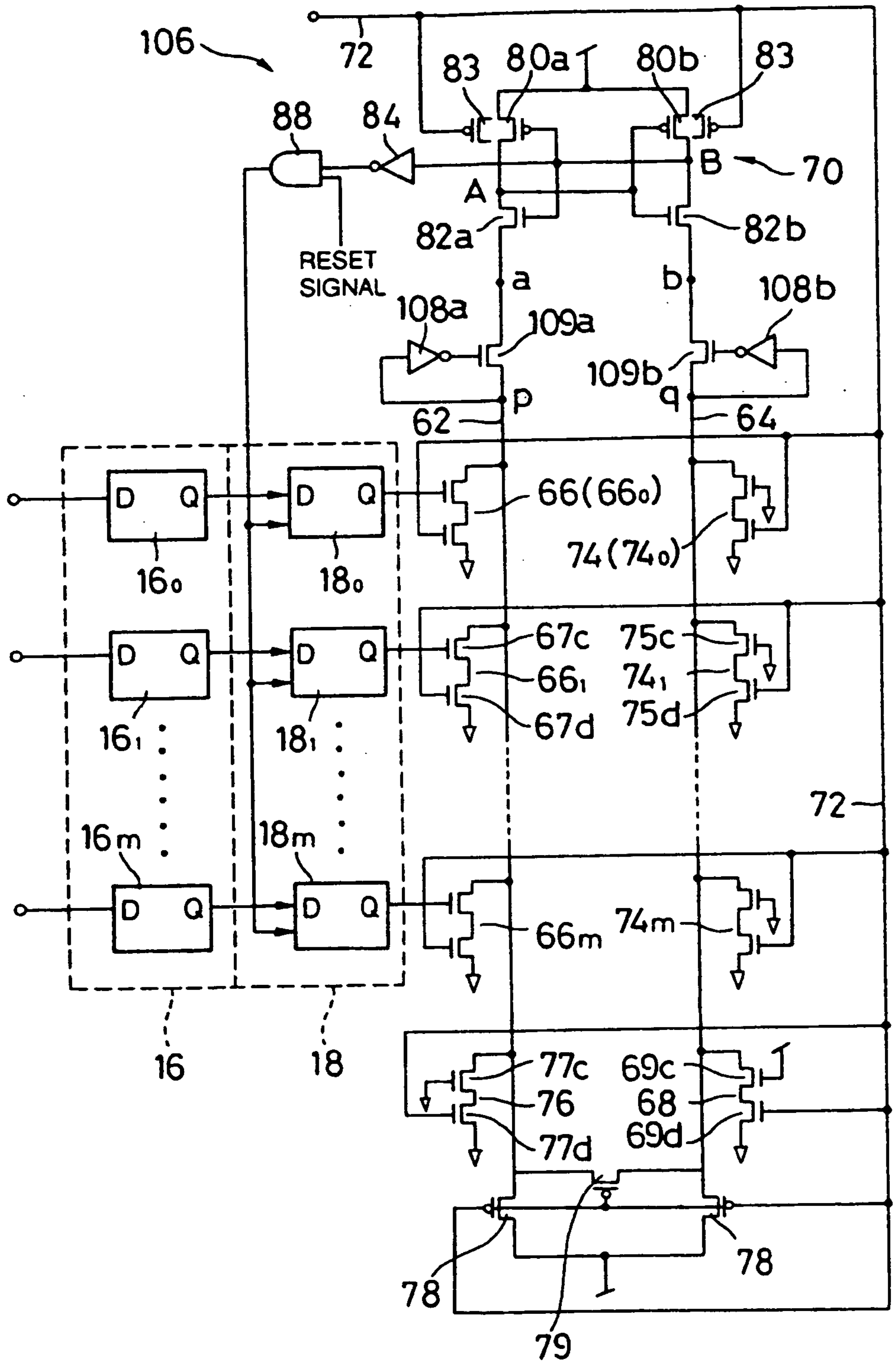

100
72
83
80a
80b
83
88
B
70
84
A
RESET SIGNAL
82a
82b
a
b
104a
103b
104b
103a
102a
102b
62
p
q
64
D Q
D Q
66(66₀)
74(74₀)
16₀
18₀
67c
75c
66₁
74₁
67d
75d
16₁
18₁
72
16m
18m
66m
74m
16
18
77c
69c
76
68
77d
69d
78
79
78

FIG. 19



106
72
83
80a
80b
83
88
84
B
70
A
82a
82b
RESET
SIGNAL
a
b
108a
109a
108b
109b
p
q
62
64
D Q
D Q
66(66₀)
74(74₀)
16₀
18₀
67c
75c
66₁
74₁
67d
75d
16₁
18₁
72
16m
18m
66m
74m
16
18
77c
69c
76
68
77d
69d
78
78
79

FIG. 20

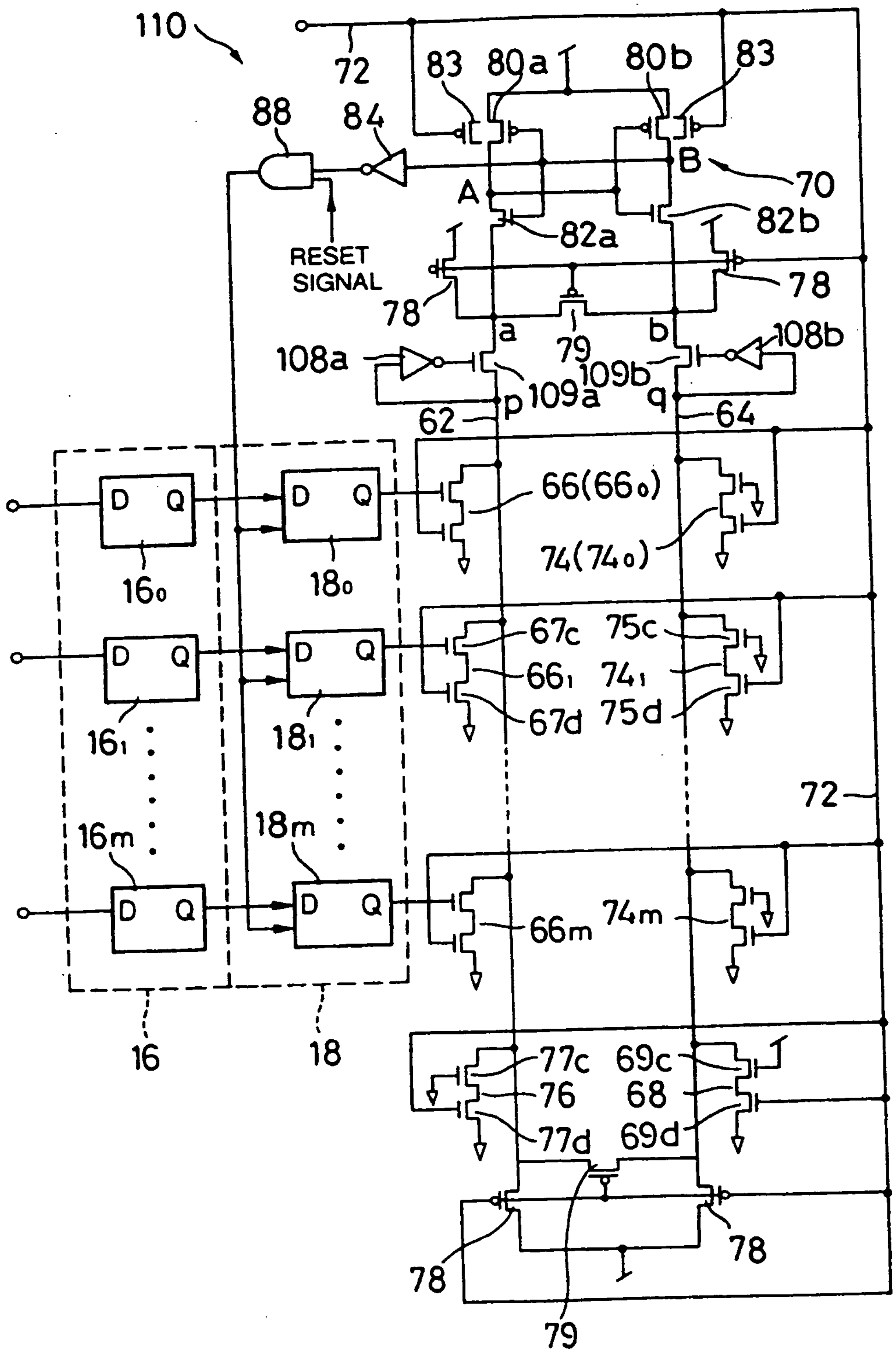

110
72
83
80a
80b
83
88
84
B
70
A
82a
82b
RESET SIGNAL
78
78
79
a
b
108a
108b
109a
109b
p
q
62
64
D Q
16₀
18₀
66(66₀)
74(74₀)
67c
75c
66₁
74₁
67d
75d
16₁
18₁
72
16m
18m
66m
74m
16
18
77c
69c
76
68
77d
69d
78
78
79

FIG. 21

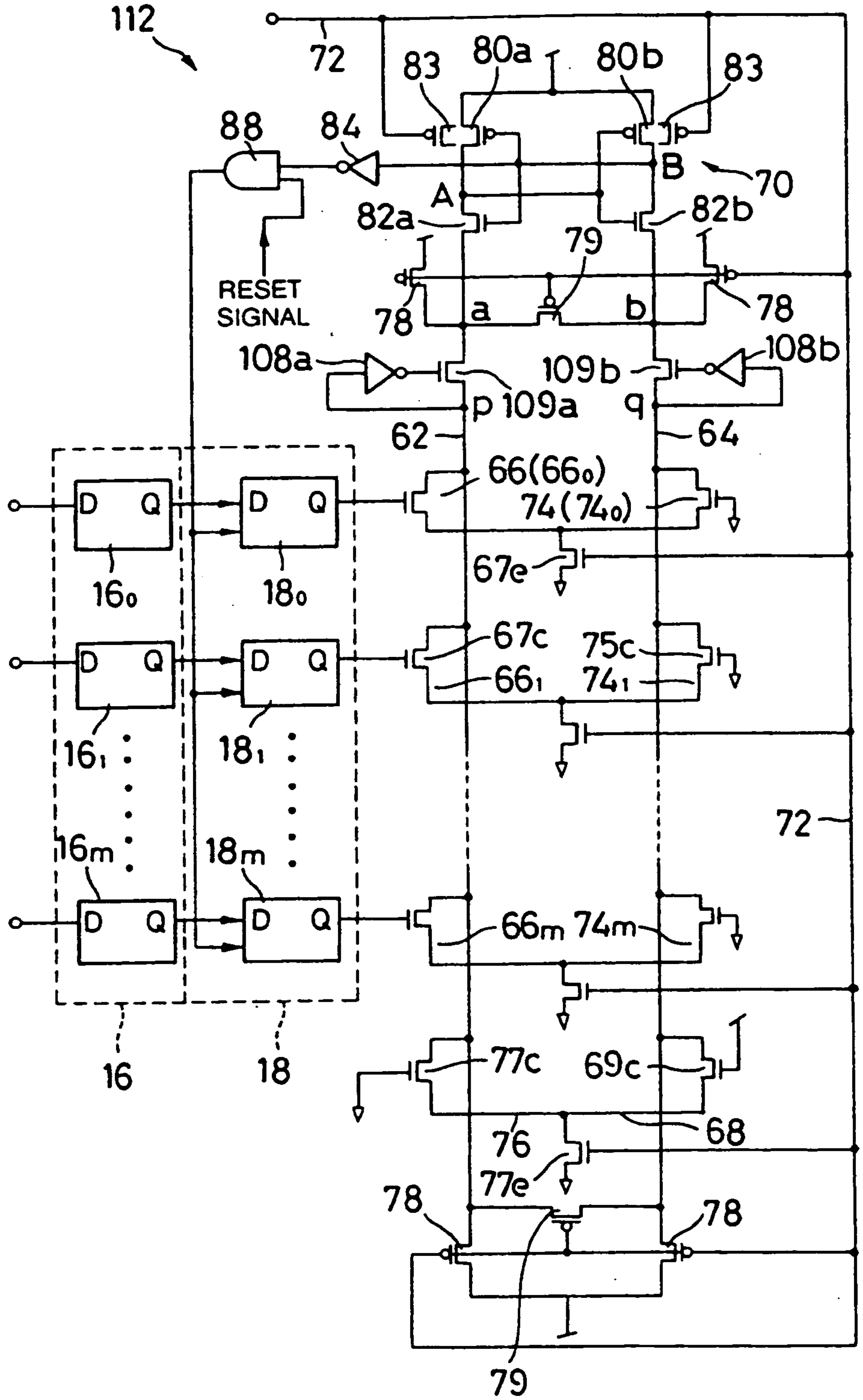

112
72
83
80a
80b
83
88
84
B
70
A
82a
82b
79
RESET SIGNAL
78
a
b
78
108a
109b
108b
p 109a
q
62
64
66(66₀)
74(74₀)
D Q
D Q
16₀
18₀
67e
67c
75c
66₁
74₁
16₁
18₁
72
16m
18m
66m 74m
16
18
77c
69c
76
68
77e
78
78
79

FIG. 22

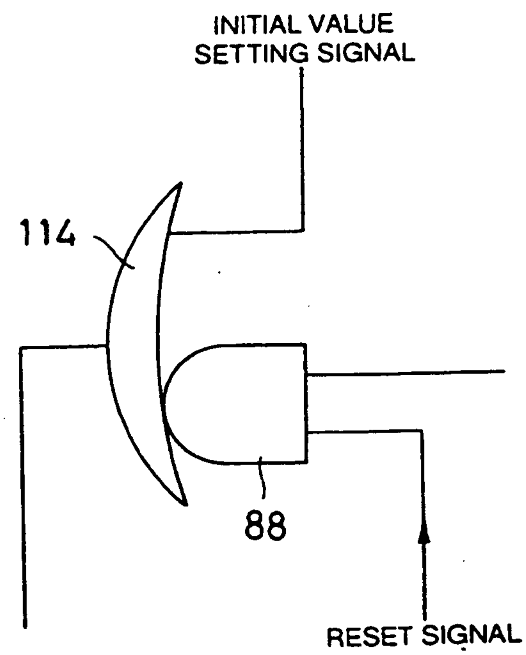


FIG. 23

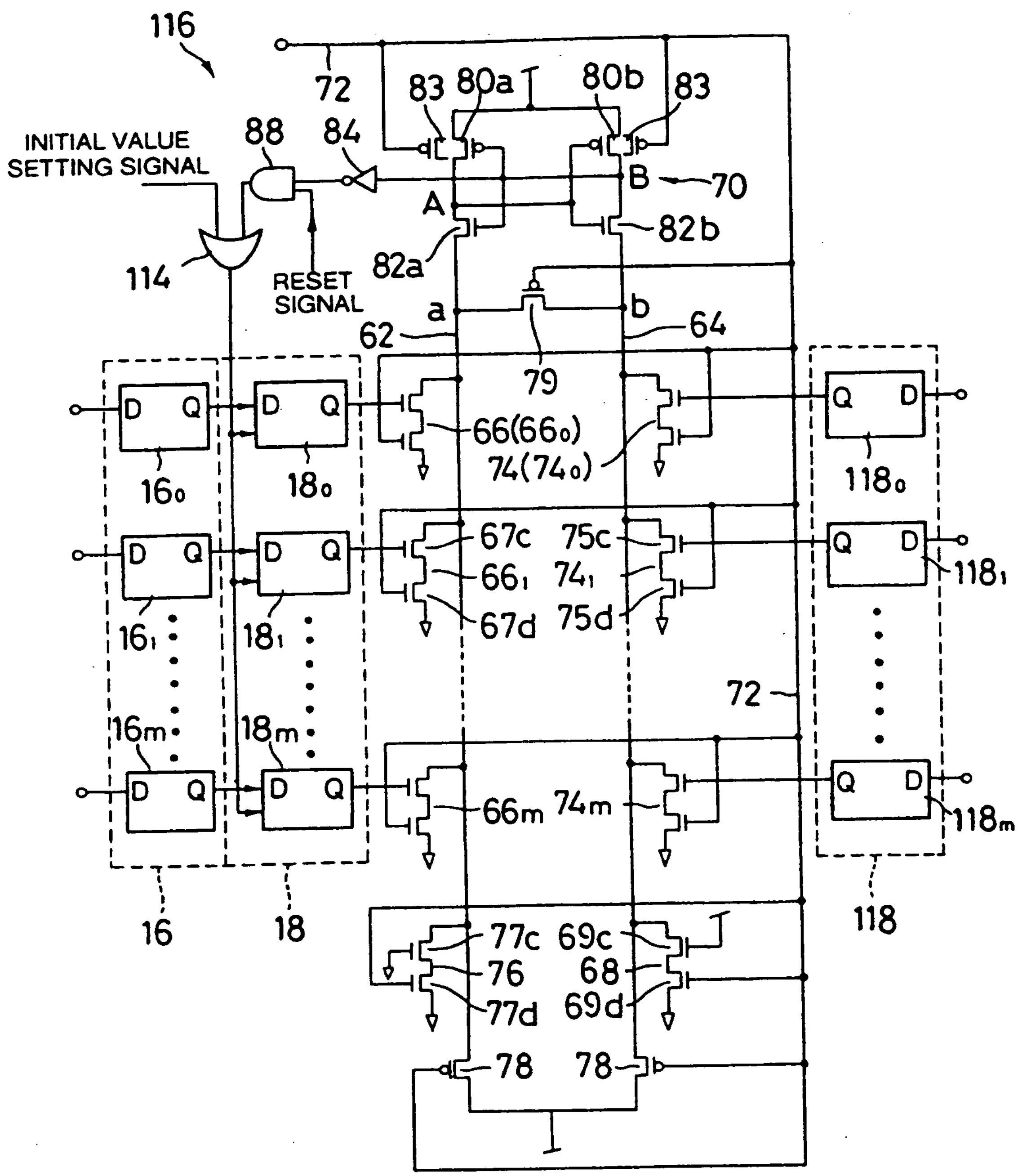

116
72
83
80a
80b
83
INITIAL VALUE
SETTING SIGNAL
88
84
B
70
A
82b
114
82a
RESET
SIGNAL
a
b
62
64
79
D
Q
16₀
18₀
66(66₀)
74(74₀)
118₀
67c
75c
66₁
74₁
118₁
16₁
18₁
67d
75d
72
16m
18m
66m
74m
118m
16
18
118
77c
69c
76
68
77d
69d
78
78

FIG. 24

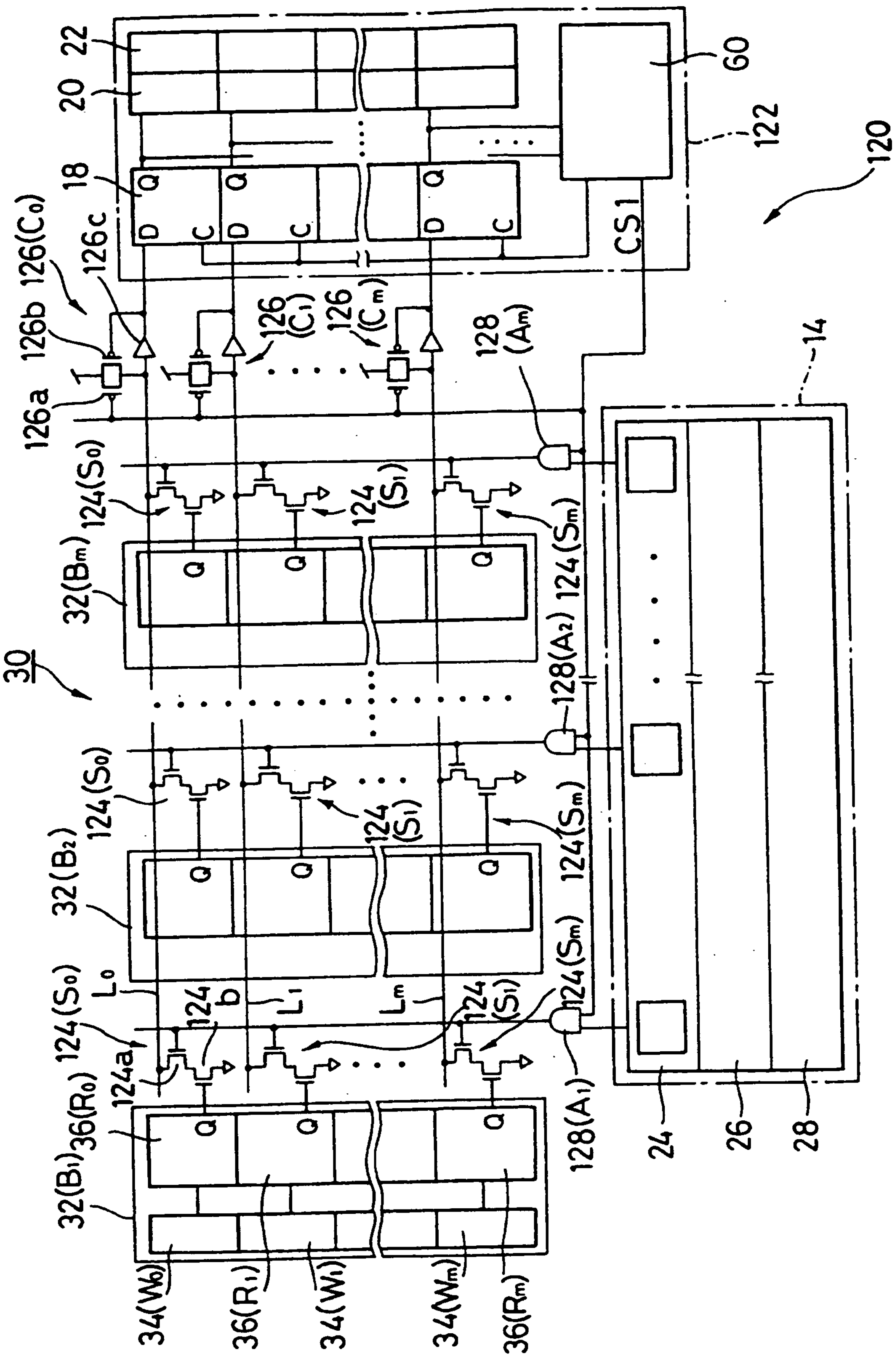

30
22
20
18
60
122
120
CS1
126(C0)
126c
126b
126a
126 (C1)
126 (Cm)
128 (Am)
14
124(S0)
124 (S1)
124(Sm)
32(Bm)
128(A2)
32(B2)
L0
L1
Lm
124a
124 b
128(A1)
32(B1)
36(R0)
34(W0)
36(R1)
34(W1)
34(Wm)
36(Rm)
24
26
28
Q
D
C

FIG. 25

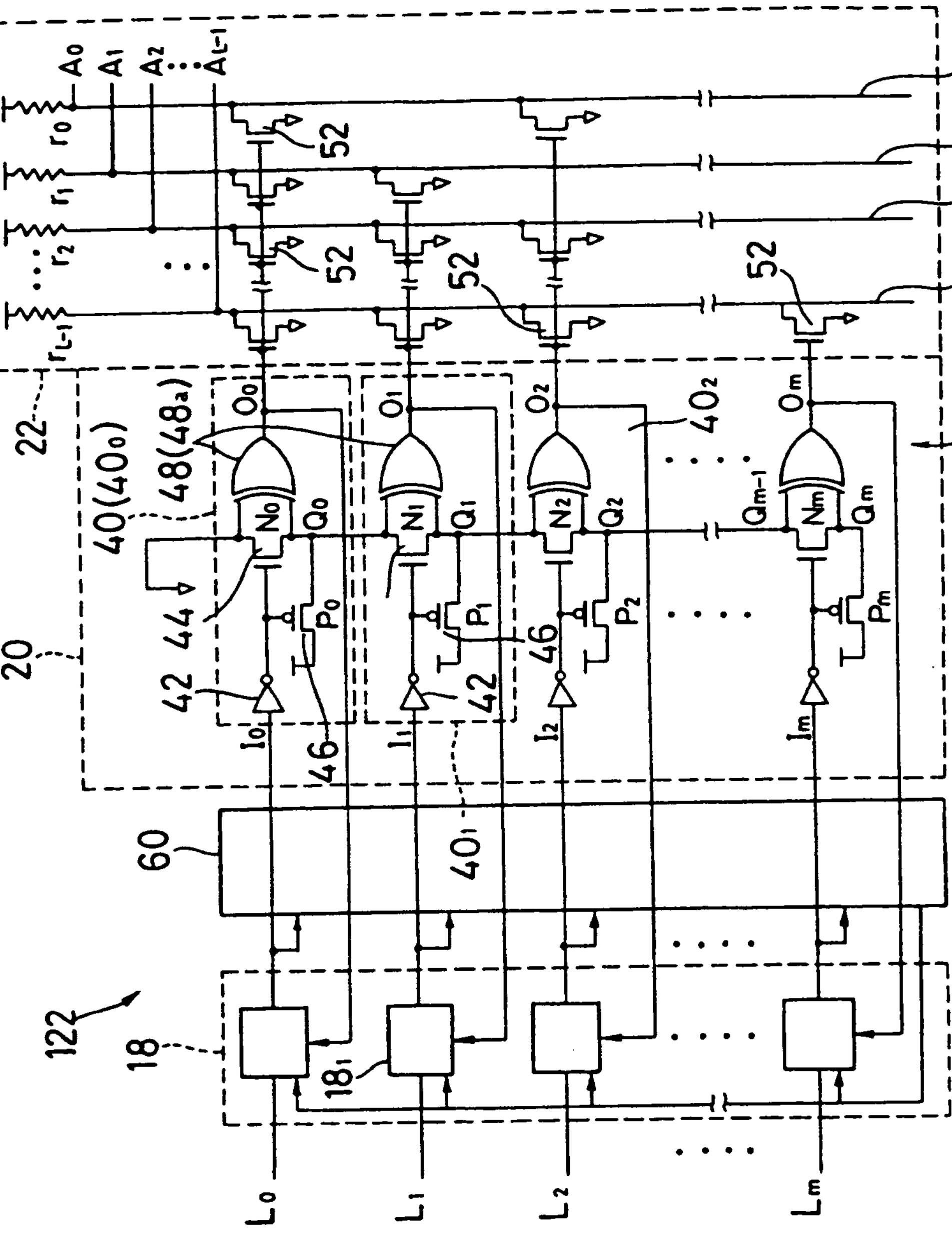

122
18
60
20
22
40(40₀)
48(48a)
42
44
46
52
40₁
40₂
40m
50₀
50₁
50₂
50L-1
L₀
L₁
L₂
Lm
I₀
I₁
I₂
Im
N₀
N₁
N₂
Nm
Q₀
Q₁
Q₂
Qm-1
Qm
P₀
P₁
P₂
Pm
O₀
O₁
O₂
Om
A₀
A₁
A₂
AL-1
r₀
r₁
r₂
rL-1
18₁

FIG. 26

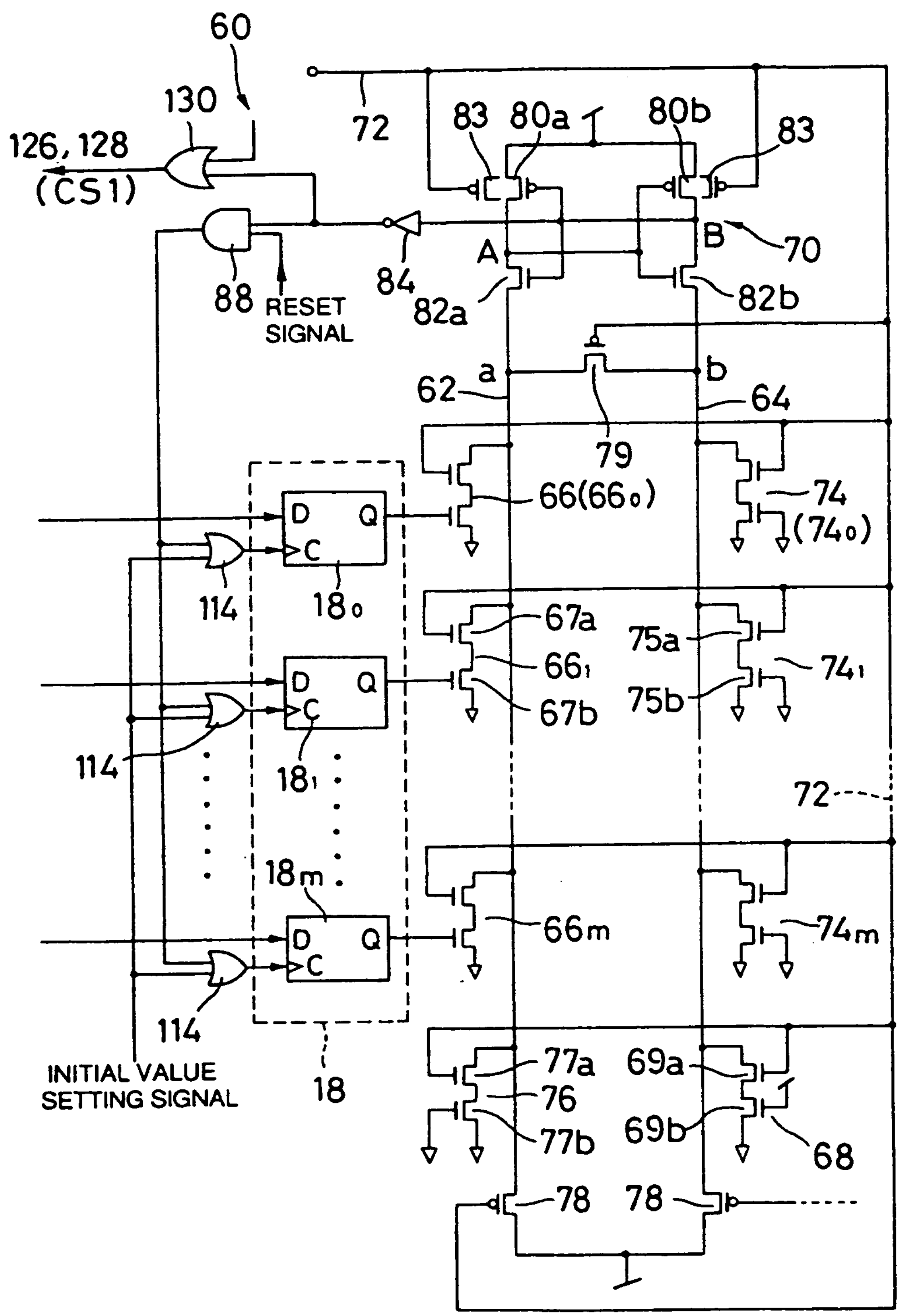

60
130
126, 128
(CS1)
72
83
80a
80b
83
70
A
B
84
88
RESET SIGNAL
82a
82b
a
b
62
64
79
66(66₀)
74
(74₀)
D
Q
C
114
18₀
67a
75a
66₁
74₁
67b
75b
114
18₁
72
18m
66m
74m
114
INITIAL VALUE SETTING SIGNAL
18
77a
69a
76
77b
69b
68
78
78

FIG. 27

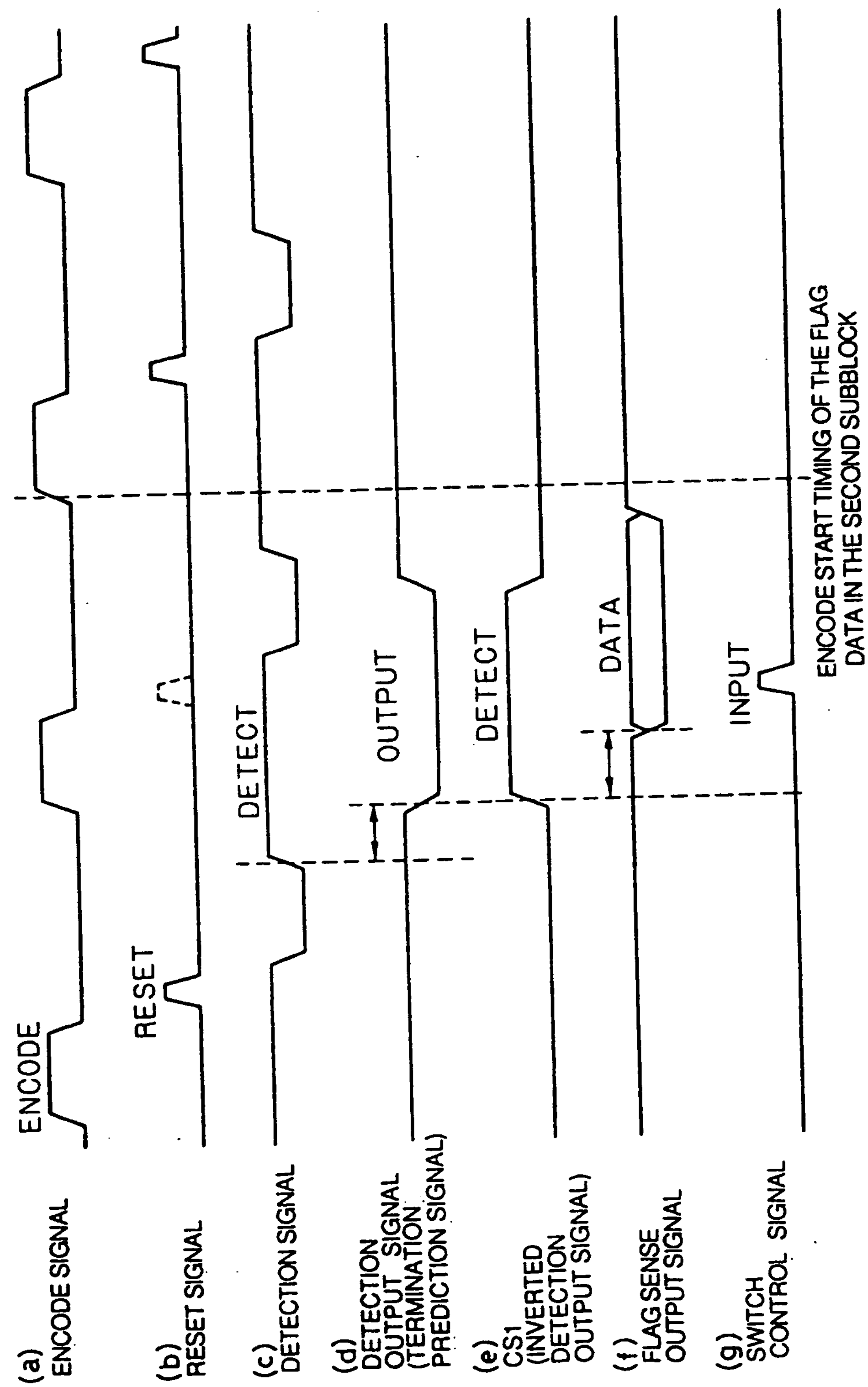

(a) ENCODE SIGNAL
(b) RESET SIGNAL
(c) DETECTION SIGNAL
(d) DETECTION OUTPUT SIGNAL (TERMINATION PREDICTION SIGNAL)
(e) CS1 (INVERTED DETECTION OUTPUT SIGNAL)
(f) FLAG SENSE OUTPUT SIGNAL
(g) SWITCH CONTROL SIGNAL
ENCODE
RESET
DETECT
OUTPUT
DETECT
DATA
INPUT
ENCODE START TIMING OF THE FLAG DATA IN THE SECOND SUBBLOCK

FIG. 28

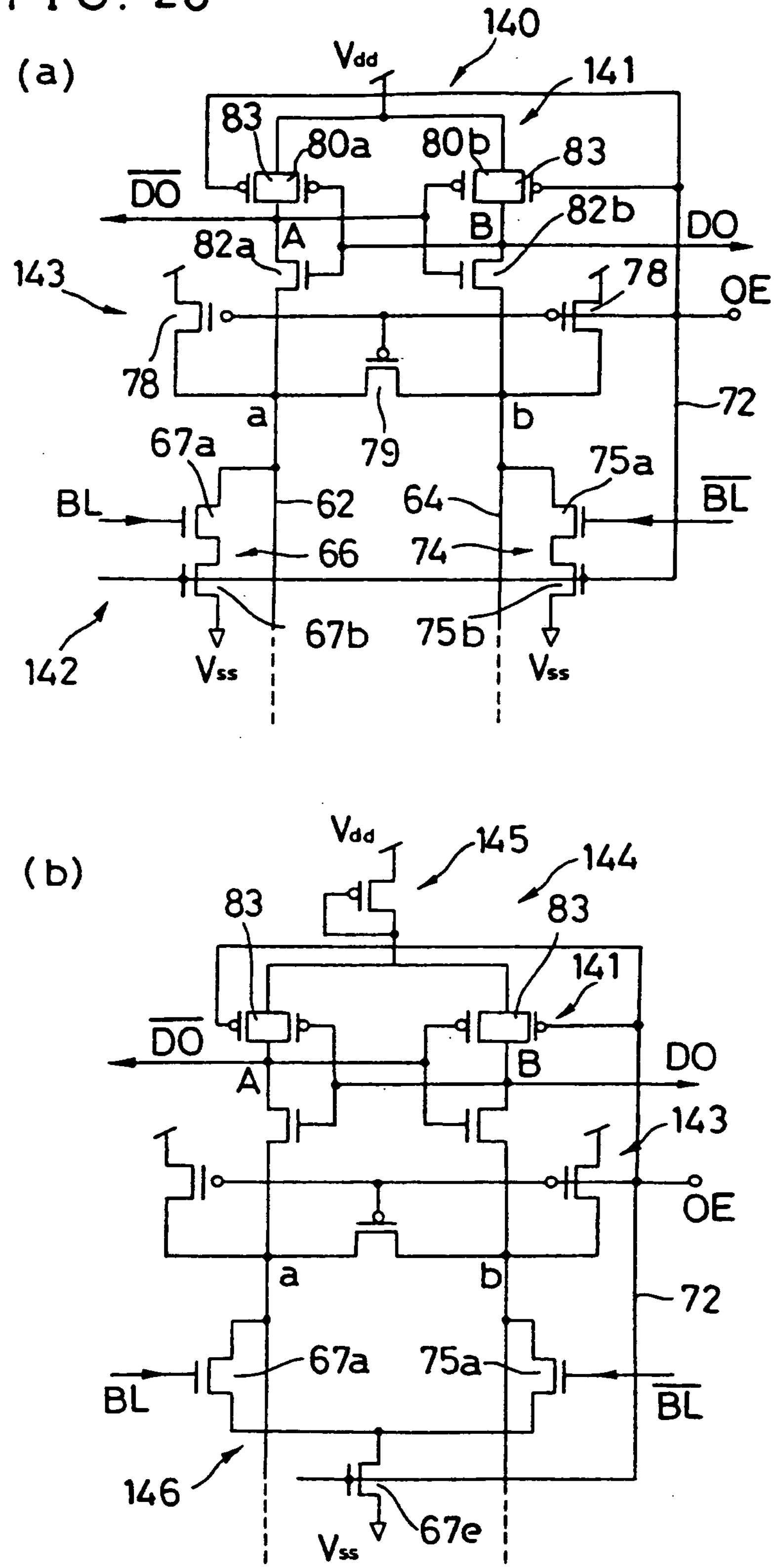
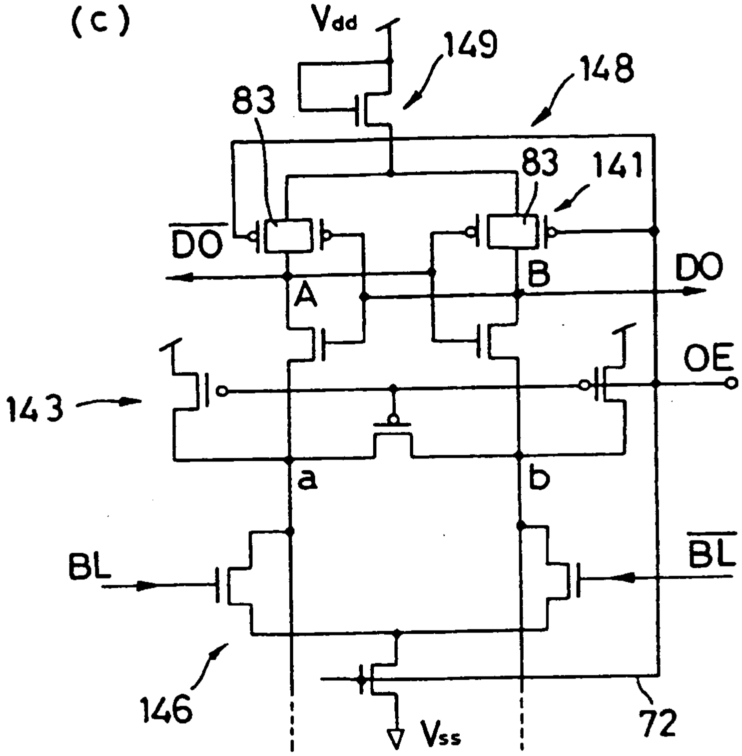

(a)
140
Vdd
141
83
80a
80b
83
DO
A
B
82b
DO
82a
143
78
OE
78
72
a
b
79
67a
75a
BL
62
64
BL
66
74
67b
75b
142
Vss
Vss
(b)
Vdd
145
144
83
83
141
DO
B
DO
A
143
OE
a
b
72
67a
75a
BL
BL
146
67e
Vss

FIG. 28

(c)


Vdd
149
148
83
83
141
DO
B
DO
A
OE
143
a
b
BL
BL
146
Vss
72

(d)

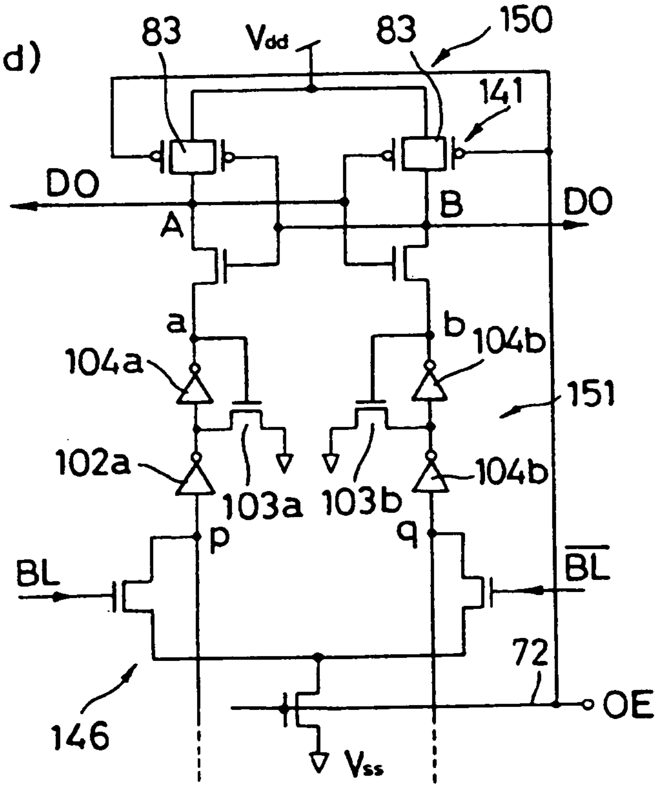
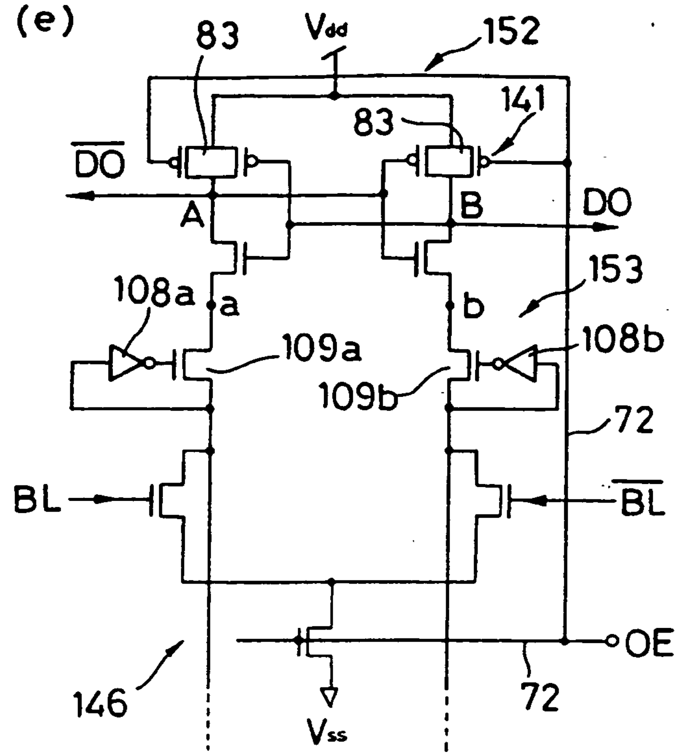

83
Vdd
83
150
141
DO
B
DO
A
a
b
104b
104a
151
102a
104b
103a
103b
p
q
BL
BL
72
OE
146
Vss

FIG. 28

(e)


83
Vdd
152
83
141
DO
A
B
DO
153
108a
a
b
109a
108b
109b
72
BL
BL
OE
146
72
Vss

(f)

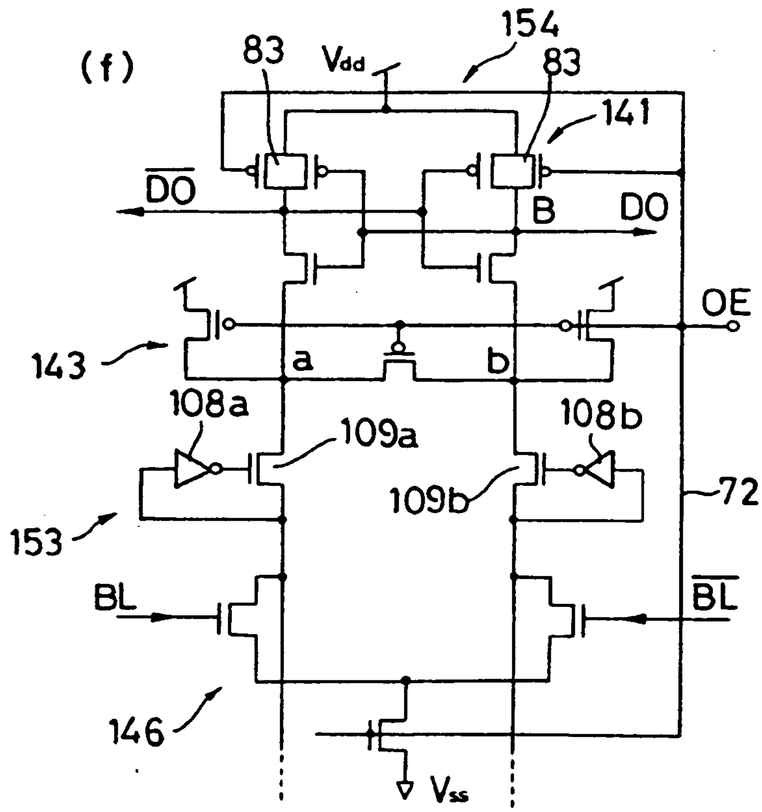
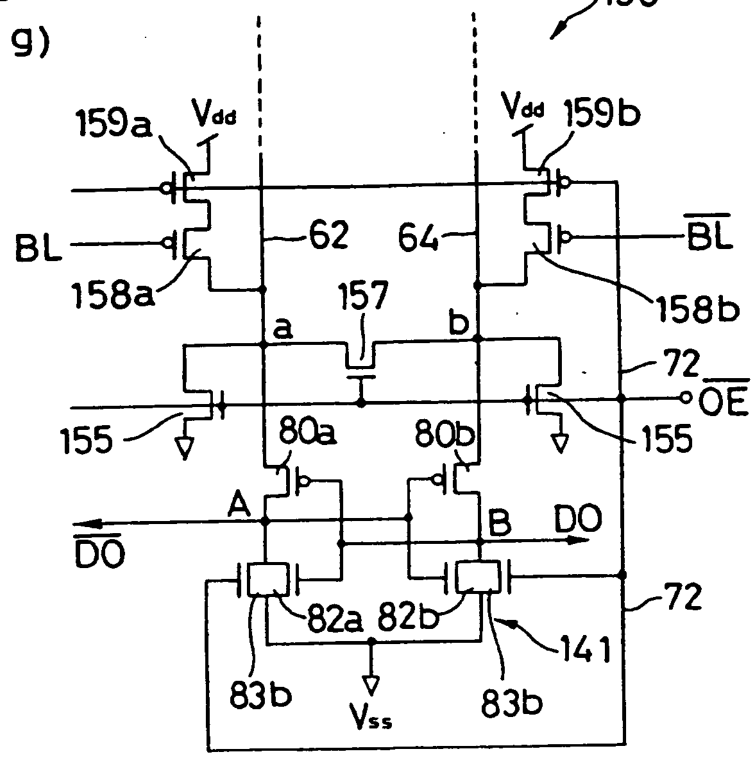

154
83
Vdd
83
141
DO
B
DO
OE
143
a
b
108a
108b
109a
109b
72
153
BL
BL
146
Vss

FIG. 28

(g)


156
159a
Vdd
Vdd
159b
BL
62
64
BL
158a
157
158b
a
b
72
OE
155
80a
80b
155
A
B
DO
DO
82a
82b
72
141
83b
Vss
83b

(h)

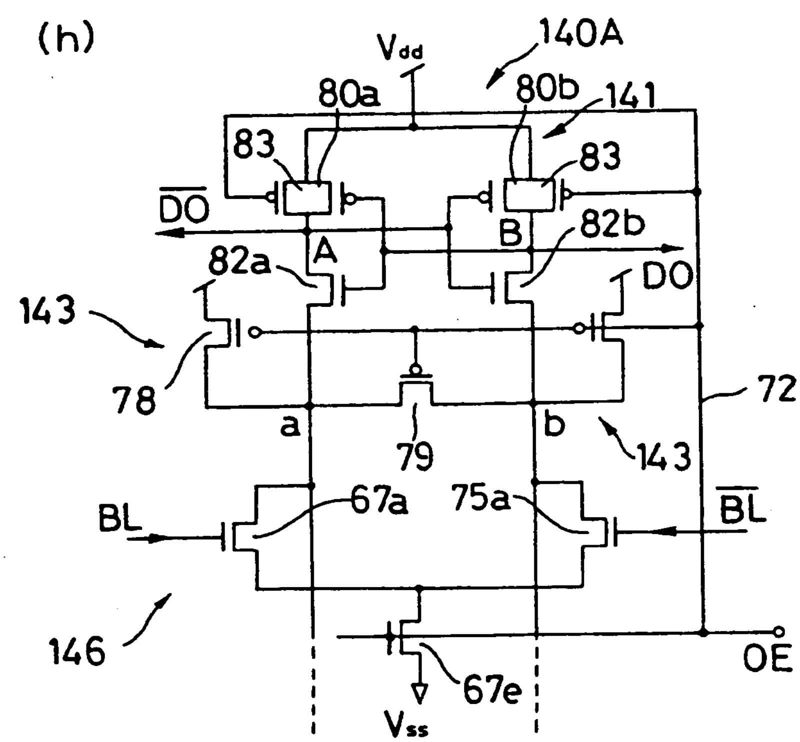

Vdd
140A
80a
80b
141
83
83
DO
B
82b
82a
A
DO
143
78
a
79
b
143
72
BL
67a
75a
BL
146
OE
67e
Vss

FIG. 29

PRIOR ART

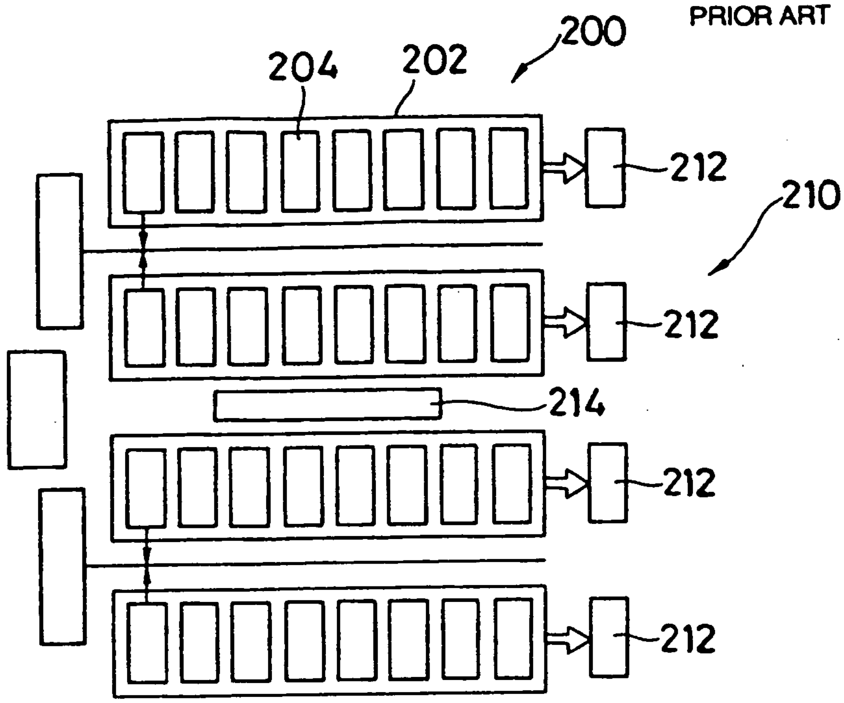


FIG. 30

PRIOR ART